Oversampling A-to-D and D-to-A Converters with Multistage Noise Shaping Modulators

KUNIHARU UCHIMURA, TOSHIO HAYASHI, TADAKATSU KIMURA, AND ATSUSHI IWATA

Abstract—**This paper proposes high resolution oversampling analog-to-digital and digital-to-analog converters. These converters utilize multistage noise shaping modulation techniques which can be implemented with VLSI MOS technology. The modulators consist of multiconnected single integration delta-sigma modulation loops. Quantization noise in the first delta-sigma loop is requantized by the next delta-sigma loop and cancelled by adding the requantized noise to the first stage signal. Quantization noise in the modulated signal is suppressed by double or multiple integration gain. Modulator resolution increases with the number of stages without feedback loop instability problems. A three-stage multistage noise shaping modulator with 1-bit quantization achieves the equivalent of 16-bit resolution for Hi-Fi audio band at 2 MHz sampling rate. Simulation results show that analog-to-digital and digital-to-analog converter circuits, constructed of switched capacitors, can be used without highly accurate components.**

I. Introduction

OVERSAMPLING analog-to-digital (A-to-D) and digital-to-analog (D-to-A) converters that employ modulation techniques, such as delta-sigma modulation [1]–[5], [15], adaptive delta modulation [6], [7], and interpolative modulation [8]–[11], reduce quantized levels by high sampling rate. They decrease both the number and variation sensitivity of analog components more effectively than conventional successive approximation converters. They can be used in combination with digital filters [12], therefore eliminating the need for precise analog pre- and postfilters. These features show that oversampling techniques are suitable for implementation using analog/digital compatible MOS VLSI and digital signal processing technologies.

However, delta-sigma modulation loop stability decreases when quantization noise is suppressed using second- or higher order integration [13], [14]. Furthermore, when analog components increase, device mismatch affects the signal-to-noise ratio (SNR) when multilevel quantization is used in such interpolative converters. Thus, these techniques cannot easily achieve the over 16-bit resolution required for Hi-Fi audio signal encoder/decoders.

This paper proposes high resolution oversampling A-to-D and D-to-A converters. These converters utilize multistage noise shaping (MASH) modulation techniques without employing higher order integrators. This paper also clarifies the suppression of baseband quantization noise by multiple high gain integration. Simulation results show that MASH modulators provide high resolution in two ways: 1) by eliminating the feedback loop instability problem caused by multiple order integrator phase shift; 2) by reducing D-to-A circuits required linearity. Analog circuit configurations suitable for VLSI implementation are also described.

Manuscript received May 13, 1987; revised April 18, 1988.

The authors are with NTT Electrical Communications Laboratories, 3-1 Morinosato Wakamiya, Atsugi, 243-01, Japan.

IEEE Log Number 8824227.

II. Multistage Noise Shaping Modulator Quantization Noise

The noise shaping modulator formed by placing a quantizer and integrators in a feedback loop removes quantization noise from the baseband by integrator gain. Using 1-bit quantization achieves high resolution and high element mismatch tolerance by reducing analog components. A double integration delta-sigma modulator is shown in Fig. 1. The bypass in Integrator-1 improves feedback loop stability. The modulated output signal V_{out} is given by the equation:

$$V_{out} = \frac{H_1 \cdot H_2 z^{-1} + H_2 z^{-1}}{(1 + H_1 \cdot H_2 z^{-1} + H_2 z^{-1})} V_{in} + \frac{Vq}{(1 + H_1 \cdot H_2 z^{-1} + H_2 z^{-1})}$$

for baseband frequencies (H_1 and $H_2 \gg 1$)

$$V_{out} \approx V_{in} + \frac{Vq}{(1 + H_1 \cdot H_2 z^{-1} + H_2 z^{-1})} \quad (1)$$

where V_{in} is the input signal, Vq is quantization noise, and H_1 and H_2 are integrator gain equal to $1/(1 - z^{-1})$. Noise in the modulated signal is suppressed by H_1 and H_2 gain. Suppression is proportional to the number of integrators. However, it is difficult to maintain feedback loop stability when more than second-order integration is used.

This paper proposes using oversampling A-to-D and D-to-A converters incorporating MASH modulation techniques. These techniques provide high resolution and eliminate the feedback loop instability problem. The two-stage MASH modulator's basic configuration is shown in Fig. 2. Each stage consists of a first-order integrator, a quantizer, and a feedback circuit. The first stage quantizes the input signal in the same way as in a conventional delta-sigma modulator. The difference between input signal and quantizer output, that is, first stage quantization noise, is

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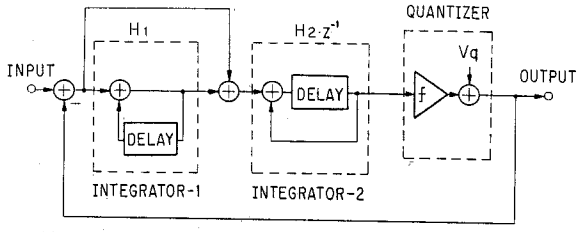

Fig. 1. Delta-sigma modulator with double integration.

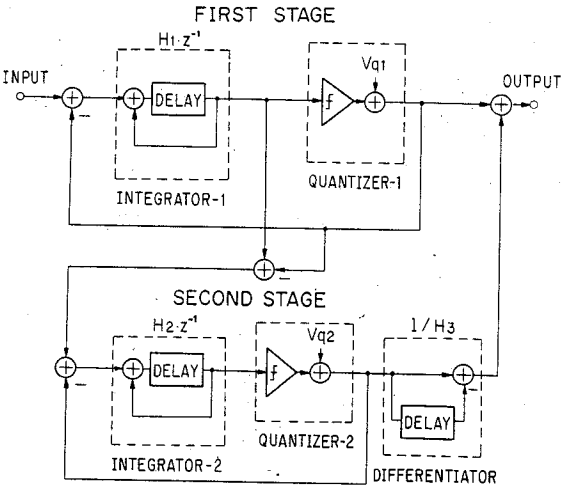

Fig. 2. Multistage noise shaping modulator with two stages.

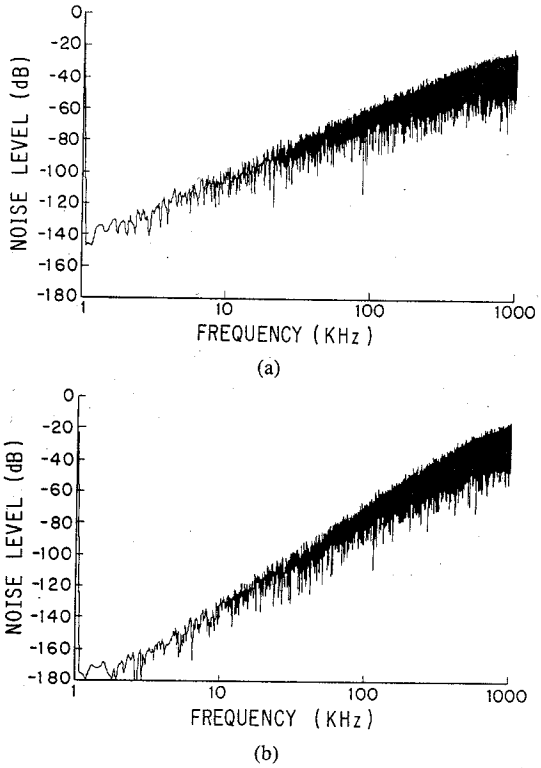

Fig. 3. Simulated quantization noise spectrum of multistage noise shaping modulator. (a) Two-stage. (b) Three-stage. Sampling rate is 2048 kHz.

accumulated by the integrator. The noise's low-frequency baseband components are amplified. Amplified noise is detected at the integrator output. The detected noise signal is requantized by the second stage. The differentiator shapes the quantizer output frequency spectrum to return it to the original signal spectrum. This signal cancels first stage quantization noise by adding it to the first stage output. If H_1 is assumed equal to H_2, the modulated output V_{out} is given by the equation:

$$V_{out} = \frac{H_1 z^{-1}}{(1 + H_1 z^{-1})} V_{in} + \frac{(H_3 - H_1) z^{-1}}{(1 + H_1 z^{-1}) H_3} Vq_1 + \frac{Vq_2}{(1 + H_1 z^{-1}) H_3}$$

for baseband frequencies ($H_1 >> 1$)

$$V_{out} \approx V_{in} + \frac{(H_3 - H_1) z^{-1}}{(1 + H_1 z^{-1}) H_3} Vq_1 + \frac{Vq_2}{(1 + H_1 z^{-1}) H_3} \quad (2)$$

where Vq_1 and Vq_2 are the quantization noise of Quantizer-1 and Quantizer-2, respectively, and $1/H_3$ is the differentiator transfer function. If H_1 is designed to equal H_3, the second term in (2) is completely cancelled and the third term is suppressed by H_1 and H_3.

The performances of A-to-D and D-to-A converters with MASH modulators have been evaluated by computer simulation. To evaluate feedback loop stability and dynamic characteristics, analog waveforms and digital bit streams were obtained by time domain simulation technique using extended Z-transform models. The required accuracy for analog components on VLSI chip were clarified by quantifying the performance degradation when nonideal models were used. The nonideal models include amplifier finite gain, dc offsets, comparator uncertainty, capacitance ratio errors, and noise sources. The quantization noise spectrum and the signal-to-noise ratio (SNR) were calculated from analog waveforms and digital bit streams by the FFT (Fast Fourier Transform) method.

The quantization noise spectrum of a two-stage MASH modulator simulated at a 2.048 MHz sampling rate is shown in Fig. 3(a). Noise is suppressed by the noise shaping characteristics of double integration. The noise spectrum slope has a 40 dB/decade gradient. The noise spectrum has the same shape as that of the double integration delta-sigma modulator. Further, second stage quantization noise is detected as the second stage integrator output, and three or more stage MASH modulators can be constructed without feedback loop instability problems. This three-stage MASH modulator makes highly effective triple integration feasible for the first time. The three-stage MASH modulator quantization noise spectrum is shown in Fig. 3(b). The slope has a 60 dB/decade gradient.

Simulated waveforms in the MASH modulator with 1-bit quantization are shown in Fig. 4. Amplitude is normalized by the maximum input level. Input waveforms of the second and third stages are exactly equal to the quantization noise of the first and second stages, respectively. Each stage output signal remains stable and does not exceed the maximum for each input signal range.

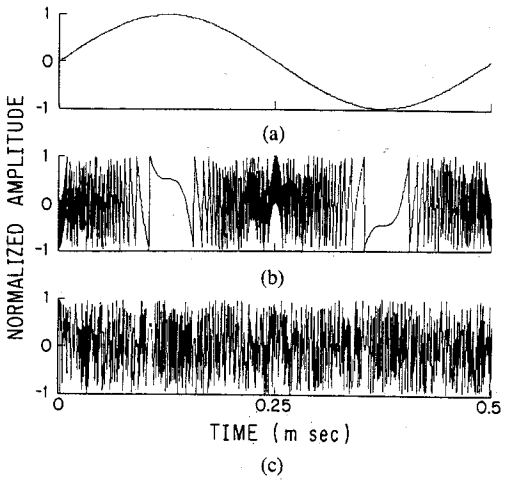

Fig. 4. Simulated waveforms in multistage noise shaping modulator. (a) First stage input. (b) Second stage input. (c) Third stage input. Quantization level is two. Sampling rate is 2048 kHz.

III. Multistage Noise Shaping Modulator Performance

In a double integration delta-sigma modulator, the integrator output amplitude increases with the input level quantizer input range. The resultant feedback loops become unstable. The effect of input sine wave amplitude on second integrator output peak levels for 1-bit quantization is shown in Fig. 5. These are simulated results where the sampling frequency is 2048 times larger than the input frequency. The 1-bit quantizer feeds back two levels that are equal to positive and negative maximum levels of the input signal centering on ground level. The input signal differences from high and low quantizer outputs become unbalanced when the input level approaches its maximum. The output of the first integrator accumulating the input differences is shaped into a triangular waveform rising or falling with the input difference magnitude. When the input differences are in heavy unbalance and the rising or falling speed is very low, the triangular waveform has a long cycle time and includes low-frequency components. In the double integration delta-sigma modulator, the second integrator amplifies the first integrator output with gain inversely proportioning to the frequency. Therefore, the second integrator output level increases rapidly with input sine wave amplitude [Fig. 5(a)], and quantization noise also increases when the second integrator output level exceeds the quantizer input range. In the two-stage MASH modulator, integrator output peak level is unaffected by input sine wave amplitude and stays within quantizer input range [Fig. 5(b)].

In the simple delta-sigma modulator, input dc-bias affects quantization noise [5]. This dependence affects the performance of A-to-D and D-to-A converters and limits their use in many applications. SNR's have been graphed for a low level −40 dB input plotted versus input dc-bias in Fig. 6(a)–(c). The quantizer has a single threshold and generates two level outputs. Fig. 6(a) shows that the simple delta-sigma modulator is greatly affected and the SNR deteriorates at many bias levels. The double integration

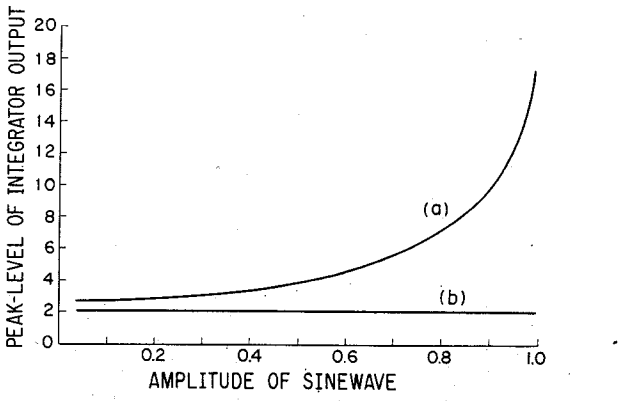

Fig. 5. Second-integrator output peak level versus input sine wave amplitude. (a) Delta-sigma modulator with double integration. (b) Multistage noise shaping modulator with two stages. Quantizer has two levels.

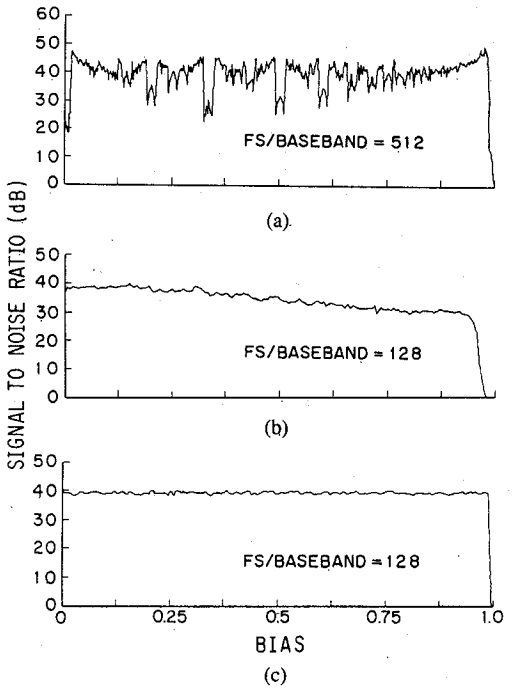

Fig. 6. Signal-to-noise ratios for a −40 dB input level and 1-bit quantization versus input bias. (a) Simple delta-sigma modulation. (b) Double integration delta-sigma modulation. (c) Two-stage MASH modulation.

delta-sigma modulator is affected only at the ends of input range [Fig. 6(b)]. Fig. 6(c) shows that the two-stage MASH modulator SNR are almost unaffected by input dc-bias. The MASH modulator can be used in the same way as a high resolution linear PCM converter over all input voltage ranges.

Feedback loop stability and sensitivity to input bias affect SNR. Simulated SNR characteristics plotted against input sine wave amplitude at 1-bit quantization and 16 kHz baseband are shown in Fig. 7. MASH modulator sampling rates are independent of the number of stages. This is because all MASH modulator feedback loop integrators operate in parallel, whereas delta-sigma modulator feedback loop integrators must operate in series. Therefore, the MASH modulator sampling rate is twice as high as the double integration delta-sigma modulator sampling rate.

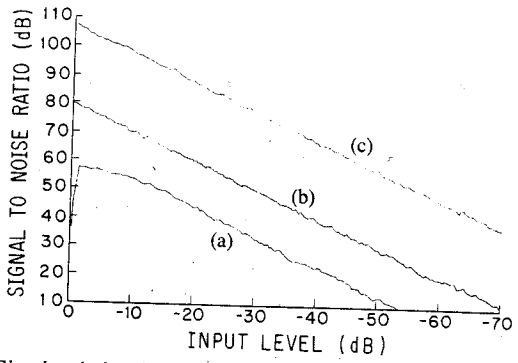

Fig. 7. Simulated signal-to-noise ratios at 1-bit quantization and 16 kHz baseband. (a) Double integration delta-sigma modulator at 1024 kHz sampling. (b) Two-stage MASH modulator at 2048 kHz sampling. (c) Three-stage MASH modulator at 2048 kHz sampling.

The SNR curve of the double integration delta-sigma modulator saturates above −10 dB [Fig. 7(a)]. The MASH modulator with SNR unaffected by input bias achieves ideal linear SNR curves [Fig. 7(b), (c)]. Fig. 7 also shows that the two-stage MASH modulator dynamic range is higher than that of the double integration delta-sigma modulator by 15 dB.

The relationship between two- and three-stage MASH modulator dynamic ranges and the ratio of sampling frequency to baseband frequency is calculated and shown in Fig. 8. Dynamic ranges increase with sampling frequency by 15 dB/octave and 21 dB/octave, respectively. The three-stage MASH modulator achieves high resolution of 16-bit at low 2 MHz sampling rate and wide 20 kHz baseband, using 1-bit quantization.

IV. MASH Modulator Circuit Configuration for A-to-D Converter

In a MASH modulator A-to-D converter, the integrators and feedback circuits can easily be implemented with switched capacitor technique. A two-stage MASH modulator suitable to MOS VLSI technology consists of two switched capacitor integrators, two 1-bit comparators, and a digital differentiator (Fig. 9). The input signal is sampled by capacitor CS1 and integrated to CI1. The quantized 1-bit signal is fed back to the input by charging a reference voltage into capacitor CD1. Analog switches and comparators are controlled by a sequence clock shown in Fig. 10. In a two-stage MASH modulator sample data model (Fig. 2), second stage input is generated from the difference of integrator and quantizer outputs. In the circuit of Fig. 9, the first stage integrator output has two phases a cycle. In the first half cycle, the integrator accumulates the input signal. In the second half cycle, it accumulates the quantized signal from the comparator. The value of the second half is equal to the difference of integrator and quantizer outputs in Fig. 2. The second stage capacitor CS2 should sample the first stage integrator output in the second half cycle.

For implementation in VLSI MOS technology, the MASH modulator must tolerate amplifier finite gain and capacitor ratio mismatch in the analog circuits. The first

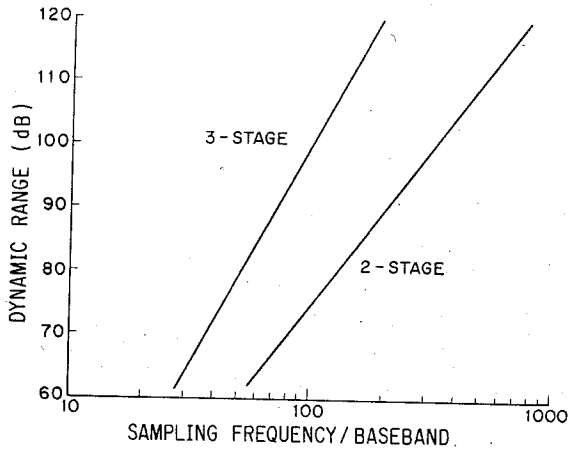

Fig. 8. Multistage noise shaping modulator dynamic range versus ratio of sampling frequency to baseband at 1-bit quantization.

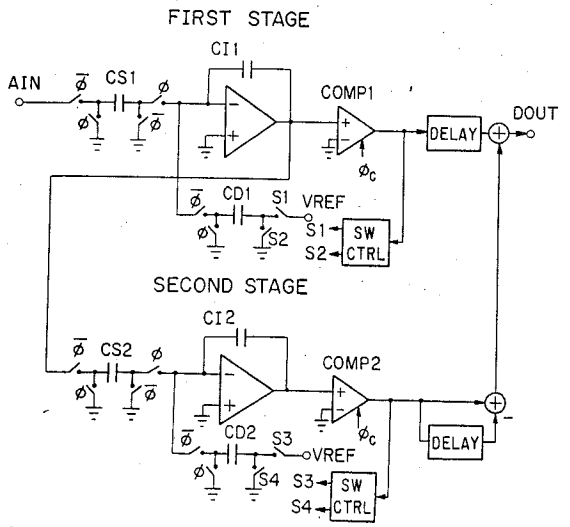

Fig. 9. Multistage noise shaping modulator circuit configuration for A-to-D converter.

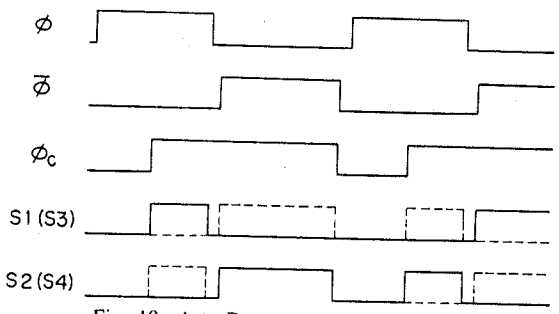

Fig. 10. A-to-D converter clock timing.

cause of SNR degradation is gain mismatch between the first and second stages. This gain mismatch is determined by the accuracy of the capacitor ratio of CS1/CD1 and CS2/CD2. Gain mismatch effects on SNR are shown in Fig. 11. To get an 80 dB dynamic range, equivalent to linear 13-bit resolution, about 5 percent gain mismatch is acceptable. Furthermore, capacitor ratio error of 1 percent achieves higher than 16-bit resolution [Fig. 11(a)]. This is because signal power transferred to the second stage is very small within the baseband, and the noise

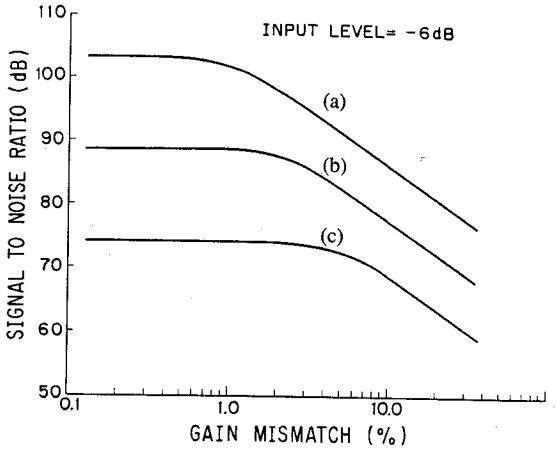

Fig. 11. Relation of gain mismatch between first and second stages to signal-to-noise ratios. Sampling frequency to baseband ratio is (a) 512; (b) 256; (c) 128.

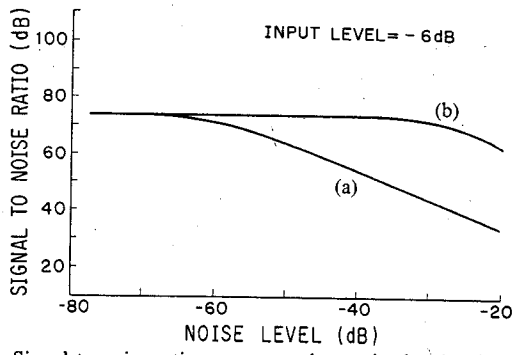

Fig. 12. Signal-to-noise ratios versus random noise level at integrator input. Noise voltages are from + VREF to −VREF at 0 dB. (a) First stage. (b) Second stage.

spectrum generated by the gain mismatch lies almost outside the baseband at the digital summing point.

The second cause of SNR degradation is circuit element noise such as MOS device $1/f$ noise, switched capacitor switching noise, and clock pulse crosstalk from digital circuits. Noise applied to integrator input is indistinguishable from the input signal or quantization noise. Fig. 12(a) shows that the integrator in the first stage must be comparatively low noise. In contrast to curve (a), curve (b) shows that the second stage is very tolerant of noise greater than 30 dB. Because the digital differentiator attenuates the second stage signal within the baseband before adding it to the first stage output, the second stage is more tolerant of circuit noise.

The third cause of SNR degradation is integrator leakage originating in amplifier finite gain. At lower frequencies, amplifier gain limits switched capacitor integrator gain. Low-frequency components of accumulated quantization noise are lost at a leakage time constant corresponding with the lower cutoff frequency. Simulated degradations caused by amplifier finite gain in the first and second stages are shown in Figs. 13 and 14. If the first stage amplifier gain is over 80 dB, SNR degradation is adequately small. Desired second stage amplifier gain is lower than first stage gain by 20–30 dB.

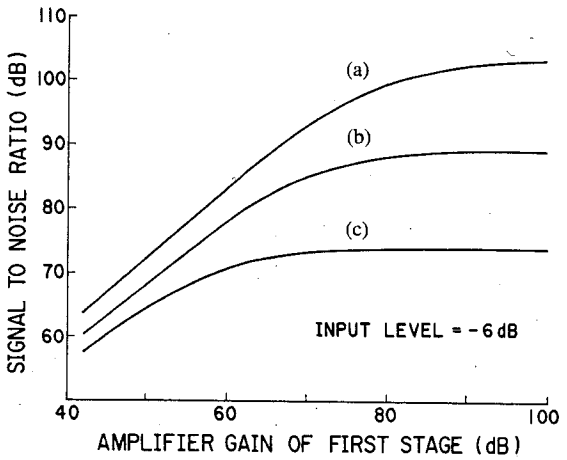

Fig. 13. Relation of first stage amplifier gain to signal-to-noise ratios. Sampling frequency to baseband ratio is (a) 512; (b) 256; (c) 128.

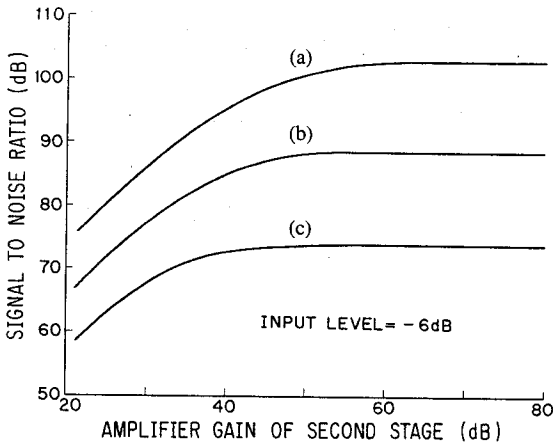

Fig. 14. Relation of second stage amplifier gain to signal-to-noise ratios. Sampling frequency to baseband ratio is (a) 512; (b) 256; (c) 128.

V. MASH Modulator Circuit Configuration for D-to-A Converter

The MASH modulator concept can be used to construct oversampling D-to-A converters. A two-stage digital MASH modulator for D-to-A converter is constructed from two digital quantizers, four digital integrators, and a differentiator as shown in Fig. 15. This configuration, where each stage has two integrators in a feedback loop, is designed for high element ratio mismatch tolerance. But feedback loop stability with two integrators is improved by reducing loop gain with a $1/4$ attenuator. When each stage has a digital integrator and a digital 1-bit quantizer in a feedback loop, the digital MASH modulator is equivalent to the reported interpolative configuration [15].

When a quantizer with three levels, 0, +1, and −1, is used in the first stage, the digital signal DOUT-1 has three levels: 0, +1, and −1. When a quantizer with two levels, +1 and −1, is used in the second stage, the second stage differentiator generates DOUT-2 having three levels: 0, +2, and −2. A 7-level local D-to-A circuit must be provided to convert these levels into the analog equivalent.

Two D-to-A conversion methods in Fig. 16 are investigated. The first method applies a binary digital signal generated by adding DOUT-1 and DOUT-2 to a conven-

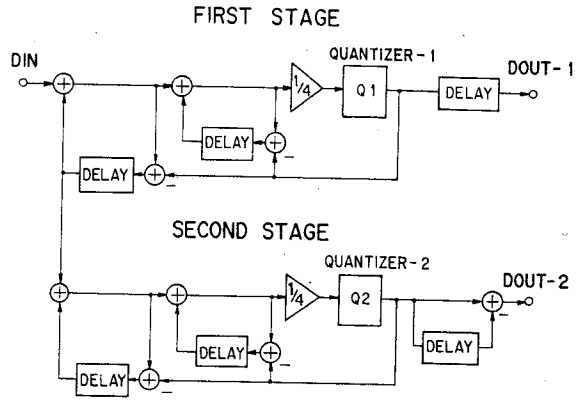

Fig. 15. Multistage noise shaping modulator configuration for D-to-A converter.

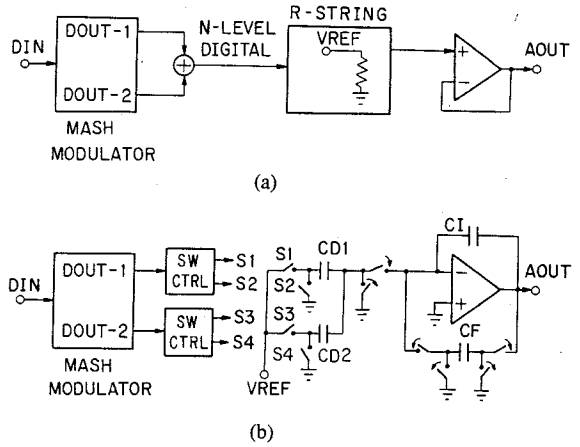

Fig. 16. (a) Conventional D-to-A conversion method using R-string circuit. (b) D-to-A conversion method using two individual switched-capacitor D-to-A circuits and an analog adder circuit.

tional D-to-A circuit, such as the dividing voltage type with resistor string [Fig. 16(a)]. The second method applies the digital signal of each stage individually to switched capacitor D-to-A circuits [Fig. 16(b)]. In this circuit, the DOUT-1 and DOUT-2 signals select CD1 and CD2 switching modes from positive charge mode, negative charge mode, and discharge mode. An amplifier with a capacitor CI adds CD1 and CD2 charges. DOUT-1 DOUT-2 signals linearity are maintained and harmonic distortion does not occur because each analog output is generated using one capacitor and one reference voltage. But conventional D-to-A circuit nonlinearity generates harmonic distortion within baseband. CD1 and CD2 capacitor ratio error causes transfer gain mismatch between the first and second stages, just as in the MASH A-to-D converter.

The D-to-A converter's (Fig. 15) SNR characteristics simulated at a 1 percent element ratio error are shown in Fig. 17. Noises include harmonic distortion and quantization noise. The dashed line shows SNR characteristics without element ratio error. Quantization noise is suppressed by first integrator high gain in the first stage and by both integrators in the second stage. These 2-stage MASH modulator SNR characteristics are almost equiv-

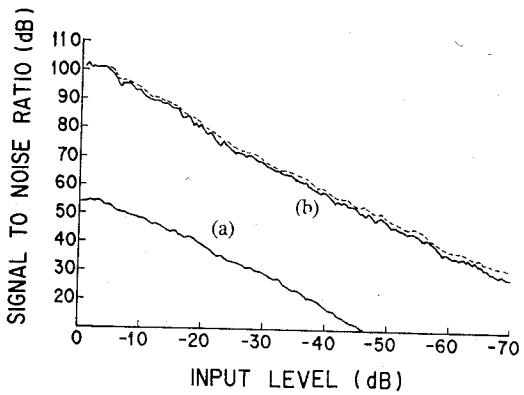

Fig. 17. Simulated D-to-A converter signal-to-noise ratios at 2048 kHz sampling and 16 kHz baseband, when element ratio error is 1 percent. (a) Using D-to-A circuit in Fig. 15(a). (b) Using D-to-A circuit in Fig. 15(b). Dashed line shows signal-to-noise ratios without element ratio error.

alent to those of the 3-stage MASH modulator constructed by the single integration delta sigma loop. Compared to the dashed line, degradation for D-to-A circuit in Fig. 16(b) is negligible [Fig. 17(b)]. But degradation for conventional D-to-A circuits is significant [Fig. 17(a)].

VI. Conclusion

This paper has proposed high resolution oversampling A-to-D and D-to-A converters utilizing multistage noise shaping modulation techniques. Multistage noise shaping modulators suppress quantization noise within baseband by double or multiple integration high gain without feedback loop instability problems. A three-stage MASH modulator with 1-bit quantization provides high resolution equivalent to 16-bit for Hi-Fi audio band at a 2 MHz sampling rate. Furthermore, the MASH modulator can be used like a high resolution linear PCM converter without being affected by input level and dc offset. Simulation results show that A-to-D and D-to-A converter circuits can be used without highly accurate components. These features are useful and suitable for high resolution digital signal processing applications in VLSI implementation.

Acknowledgment

The authors wish to thank H. Mukai, T. Sudo, and E. Arai of the Electrical Communications Laboratories for their encouragement throughout this work.

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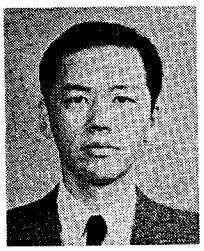

Kuniharu Uchimura was born in Kagoshima, Japan, on January 23, 1954. He received the B.S. degree in electronic engineering from Kagoshima University, Kagoshima, Japan, in 1976.

In 1976 he joined the Electrical Communications Laboratories, Nippon Telegraph and Telephone Corporation, Musashino, Tokyo, Japan. He has been engaged in the research and design of CMOS logic LSI's and analog/digital compatible LSI's for communication use. His recent work is in VLSI A-to-D and D-to-A converters. He is currently with NTT Electrical Communications Laboratories, Atsugi, Japan.

Mr. Uchimura is a member of the Institute of Electronics, Information, and Communication Engineers of Japan.

Toshio Hayashi was born in Toyama, Japan, on January 14, 1951. He received the B.S. and M.S. degrees in electronic engineering from Nagoya Institute of Technology, Japan, in 1973 and 1975, respectively.

He joined NTT Electrical Communications Laboratories in 1975. He has been engaged in research and the design of high-speed bipolar-memory LSI's. He is now engaged in the research and development of analog LSI's for communication use.

Mr. Hayashi is a member of the Institute of Electronics, Information, and Communication Engineers of Japan.

Tadakatsu Kimura was born in Hokkaido, Japan, on August 20, 1947. He received the B.S. degree in engineering from Muroran Institute of Technology, Muroran, Japan, in 1968.

He joined NTT Electrical Communications Laboratories in 1968. From 1968 to 1970 he researched hybrid integration circuits, such as stripline circuit and microwave amplifiers. From 1971 to1974 he was engaged in developmental research on high-speed hybrid integration circuit for PCM coaxial transmission-system repeaters. He is now engaged in research on CMOS LSI for digital processing and analog LSI's for subscriber line interface circuits.

Mr. Kimura is a member of the Institute of Electronics, Information, and Communication Engineers of Japan.

Atsushi Iwata was born in Nagoya, Japan, on January 14, 1946. He received the B.S. and M.S. degrees in electronic engineering from Nagoya University, Nagoya, Japan, in 1968 and 1970, respectively.

He joined the Electrical Communications Laboratories, Nippon Telegraph and Telephone Corporation, Tokyo, Japan, in 1970. He has been engaged in the research and design of analog/digital VLSI's for high speed and high accuracy signal processing. He is currently with NTT Electrical Communications Laboratories, Atsugi, Japan.

Mr. Iwata is a member of the Institute of Electronics, Information, and Communication Engineers of Japan.