IEICE TRANS. ELECTRON., VOL. E81–C, NO. 1 JANUARY 1998

PAPER *Special Issue on Technology Challenges for Single Electron Devices*

A Stochastic Associative Memory Using Single-Electron Tunneling Devices

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SUMMARY This paper proposes a new associative memory architecture using stochastic behavior in single electron tunneling (SET) devices. This memory stochastically extracts the pattern most similar to the input key pattern from the stored patterns in two matching modes: the voltage-domain matching mode and the time-domain one. In the former matching mode, ordinary associative memory operation can be performed. In the latter matching mode, a purely stochastic search can be performed. Even in this case, by repeating numerous searching trials, the order of similarity can be obtained. We propose a circuit using SET devices based on this architecture and demonstrate its basic operation with a simulation. By feeding the output pattern back to the input, this memory retrieves slightly dissimilar patterns consecutively. This function may be the key to developing highly intelligent information processing systems close to the human brain.

key words: *associative memory, single-electron tunneling, SET, single-electron transistor*

1. Introduction

A number of studies about associative memory have been conducted. In digital VLSI, content-addressable memory (CAM), which is a kind of associative memory, has been developed and used in practical applications [1]. In conventional analog circuits, a compact associative memory circuit was proposed using *neuron MOS transistors* [2]. Other approaches arose from artificial neural network research. One led to the *associatron*, a historical neural network model of associative memory [3], and another is related to a symmetrically-connected neural network model proposed by J.J. Hopfield [4], [5].

All the associative memories proposed so far achieve *deterministic* association; the same initial state leads to the same result. In associations performed in the human brain, however, different results are often obtained from the same initial state. This may be described as chaotic behavior in highly nonlinear systems [6]. In this paper, we propose another model and architecture of such associative memory, based on a purely stochastic behavior of quantum mechanical phenomena in single-electron tunneling (SET) devices.

New architectures and circuits using SET devices have been actively proposed recently [7]–[9]. However, most approaches are based on the idea of replacing conventional MOS devices, which operate deterministically, with SET devices. One idea uses the unique features of SET devices effectively by utilizing stochastic behavior in generating random operations in Boltzmann machine neurons [10]. A similar stochastic operation is also achieved in the circuit which we propose in this paper.

In Sect. 2, we propose a basic idea and an architecture featuring new stochastic associative memory. In Sect. 3, an example of the stochastic associative memory circuits is proposed, and two operation modes are described. In Sect. 4, the basic operation is demonstrated with some simulation results. In Sect. 5, our discussion is developed and our conclusion is derived in the last section.

2. Basic Model and Architecture

Let an associative memory device be defined as one that extracts similar patterns to the key pattern Ψ from stored patterns Φ_k $(k = 1, \cdots, M)$, where Ψ is given by the external system, and Φ_k are stored in the device. All patterns consist of N bit binary data:

$$\Psi = \{\xi_j;\ j = 1, \cdots, N\}, \tag{1}$$

$$\Phi_k = \{\zeta_{jk};\ j = 1, \cdots, N,\ k = 1, \cdots, M\}, \tag{2}$$

$$\xi_j \in \{0, 1\},\ \zeta_j \in \{0, 1\}. \tag{3}$$

Here, let us define ν_k as the number of unmatched bits between Ψ and Φ_k, and k_1 as the suffix of the most similar Φ_k to Ψ, which means that $\nu_{k_1} < \nu_k$, $^\forall k \neq k_1$, and k_2 as that of the second, and so on; i.e.,

$$\nu_{k_1} \leqq \nu_{k_2} \leqq \nu_{k_3} \leqq \cdots. \tag{4}$$

The proposed associative memory stochastically extracts Φ_{k_1}. It sometimes extracts Φ_{k_2} or Φ_{k_3} and so on. However, if we define the probabilities of extracting Φ_k as P_k, we can expect

$$P_{k_1} \geqq P_{k_2} \geqq P_{k_3} \geqq \cdots. \tag{5}$$

By repeating numerous extraction trials, we can obtain the order of k in similarity; i.e. $k_1, k_2, k_3, \cdots$. Furthermore, the memory can extract all patterns of which the

Manuscript received June 2, 1997.
Manuscript revised September 8, 1997.

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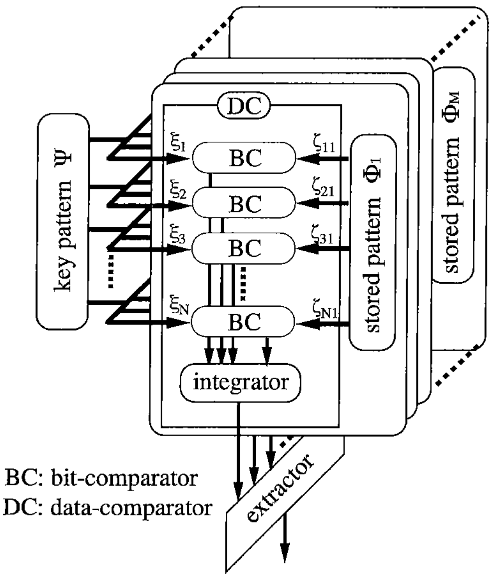

Fig. 1 Associative memory architecture.

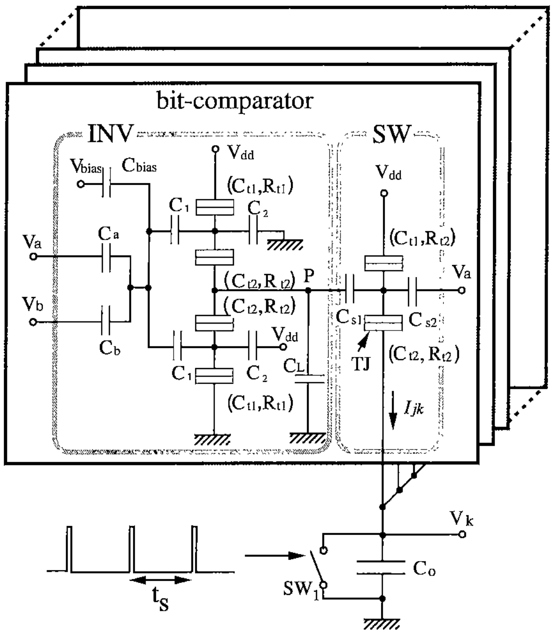

Fig. 2 Data-comparator circuit.

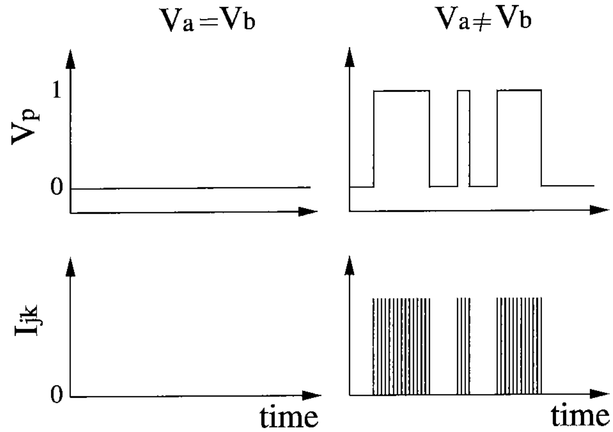

Fig. 3 Schematic figure for explaining the relation between V_p and I_{jk}. We assume $V_a = 1$.

Hamming distance is less than the given value. These are the unique characteristic of the proposed device.

This associative memory has M *data-comparators* and an *extractor*. Each data-comparator has N *bit-comparators* as shown in Fig. 1. Each data-comparator unifies the results from the bit-comparators, the extractor unifies the results from all the data-comparators, and finally this memory outputs the decision result of the extractor.

3. Circuits and Operation

First, bit-level comparisons between Ψ and Φ_k are performed at all bit-comparators in each data-comparator in parallel. If $\xi_j = \zeta_{jk}$, then the binary output of the j-th bit-comparator is "0." Otherwise it stochastically oscillates between $\{0, 1\}$.

Figure 2 shows an example of the data-comparator including bit-comparator circuits composed of SET devices. The bit-comparator circuit consists of two-input CMOS-type SET inverter INV [8], [10] and two-input SET switch SW. Here, let I_{jk} be defined as the output current of the bit-comparator associated with electrons passing through SET device TJ. By adjusting the device parameters, this circuit operates as follows.

Input voltages V_a and V_b correspond to data bits ξ_j and ζ_{jk}, respectively. If $V_a = V_b$, then the voltage of node P, V_P, is always $\overline{V_a}$. Output current I_{jk} is zero in this case. If $V_a \neq V_b$, then an electron goes in and out of node P at random; that is V_P oscillates. Current I_{jk} oscillates accompanying electrons passing through TJ when $V_P = V_a$. Figure 3 schematically shows this situation. The frequency and duty-ratio of the oscillations are related to the probability of the electron transition and depend on the device parameters.

Next, all current outputs I_{jk} of bit-comparators are summed up at capacitor C_o and each data-comparator outputs the result as a voltage. Since capacitor C_o is shorted at intervals of sampling time t_s by switch SW_1, output voltage V_k at the end of each interval is

$$V_k = \frac{1}{C_o} \sum_{j=1}^{N} \int_0^{t_s} I_{jk}(t)dt, \tag{6}$$

where C_o is set proportionally to t_s in order to obtain an appropriate voltage of V_k. If $\Psi = \Phi_k$; i.e., $\xi_j = \zeta_{jk}, \forall j$, then obviously $V_k = 0$. When $\Psi \neq \Phi_k, \forall k$, in order to extract the most similar pattern, we propose the following two methods.

3.1 Matching in Voltage Domain

If we set t_s longer than the average period of the oscillation in V_p, V_k is statistically proportional to the number of unmatched bits, ν_k, in the voltage domain. Thus, the order of similarity in Φ_k, k_i, expressed in Eq. (4), can statistically be obtained by comparing V_k with the ramping reference voltage as in conventional analog sorting circuits [2].

The fluctuation of V_k decreases when making t_s long. If t_s is long enough, the order of similarity can be obtained almost deterministically, which is the same as with ordinary associative memory. In contrast, if t_s is set in the order of the average period of the oscillation, the fluctuation of V_k is very large and association becomes stochastic.

3.2 Matching in Time Domain

If we set t_s shorter than the average period of the oscillation in V_p, V_k also oscillates, and there exist sampling intervals during which $V_k = 0$. The average span between the sampling events at which $V_k = 0$ statistically increases with increases in ν_k because $V_k = 0$ only if $I_{jk} = 0$ for all j. Thus, if the output of the k_i-th data-comparator V_{k_i} becomes zero earliest in the consecutive sampling intervals, our associative memory extracts Φ_{k_i}. The probability that Φ_{k_i} is most similar to Ψ is a maximum in this case.

Let us estimate the time dependence of the probability of detecting $V_k = 0$ in the sampling events with a parameter of ν_k. Consider a bit-comparator with different inputs and its typical V_p change as shown in Fig. 4, where $V_a = 1$ is assumed; therefore, $I_{jk} \neq 0$ when $V_p = 1$, and vice versa. We define T and a as the average period and the ratio of the interval when $V_p = 0$ in oscillation of V_p, respectively.

When a sampling event starts within the time span of $aT - t_s$, I_{jk} is always zero in this sampling interval. Since the relation between V_p oscillation and sampling timing is random, the probability that I_{jk} is always zero in a sampling interval is statistically estimated at

$$prob_{jk} = \frac{aT - t_s}{T} = a - \frac{t_s}{T}. \tag{7}$$

In a data-comparator, the probability of detecting $V_k = 0$ is statistically estimated at

$$prob_k = \left(a - \frac{t_s}{T}\right)^{\nu_k}. \tag{8}$$

The probability that V_k becomes zero at time t for the first time is

$$prob_k(t) = \left[1 - \left(a - \frac{t_s}{T}\right)^{\nu_k}\right]^{\frac{t}{t_s}} \left(a - \frac{t_s}{T}\right)^{\nu_k}. \tag{9}$$

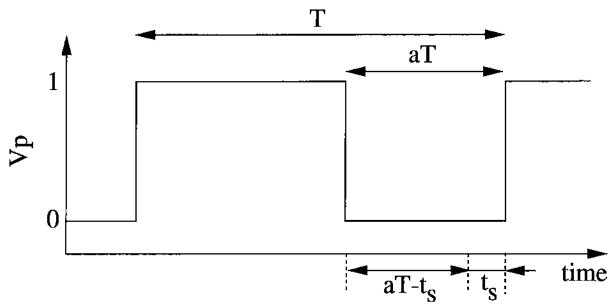

Fig. 4 Schematic figure introducing the probability of detecting $I_{jk} = 0$. We assume $V_a = 1$.

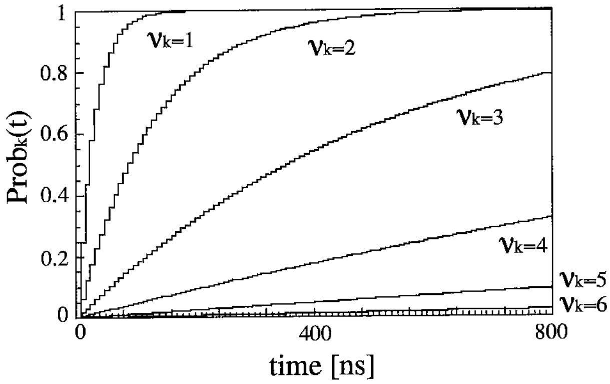

Fig. 5 Time dependence of $P_k(t)$ with a parameter of ν_k.

Thus, the probability that V_k becomes zero at least once by time t is

$$Prob_k(t) = \sum_{j=0}^{n-1} \left[1 - \left(a - \frac{t_s}{T}\right)^{\nu_k}\right]^j \left(a - \frac{t_s}{T}\right)^{\nu_k}, \tag{10}$$

$$n = t/t_s \geqq 1. \tag{11}$$

Figure 5 shows the time dependence of $Prob_k(t)$ with a parameter of ν_k, where $T = 36$ nsec, $a = 0.5$, $t_s = 8$ nsec. Thus, it is confirmed from Fig. 5 that the order of similarity in Φ_k, k_i expressed in Eq. (4), is stochastically obtained in the time domain.

4. Simulation Results

We developed a simulator for SET circuits based on Refs. [9], [11]. Figure 6 shows the simulation results about the dependence of I_{jk} on $V_{a,b}$ in the bit-comparator. It can be seen that I_{jk} oscillates randomly when $V_a \neq V_b$. The black areas indicate that I_{jk} oscillates at a high frequency, which is the effect of electrons passing through the switch SW. In this simulation, parameters were: $V_{dd} = 6.5$ mV, $V_{bias} = 2.3$ mV, $C_a = 55$ aF, $C_b = 55$ aF, $C_{bias} = 10$ aF, $C_1 = 6$ aF, $C_2 = 9$ aF, $C_{s1} = 10$ aF, $C_{s2} = 9$ aF, $C_{t1} = 1$ aF, $C_{t2} = 2$ aF, $C_L = 22$ aF, $R_{t1} = 45$ MΩ, $R_{t2} = 1$ MΩ, *temperature* = 1 mK.

Figure 7 shows the waveforms of I_{jk} when $\xi_j \neq$

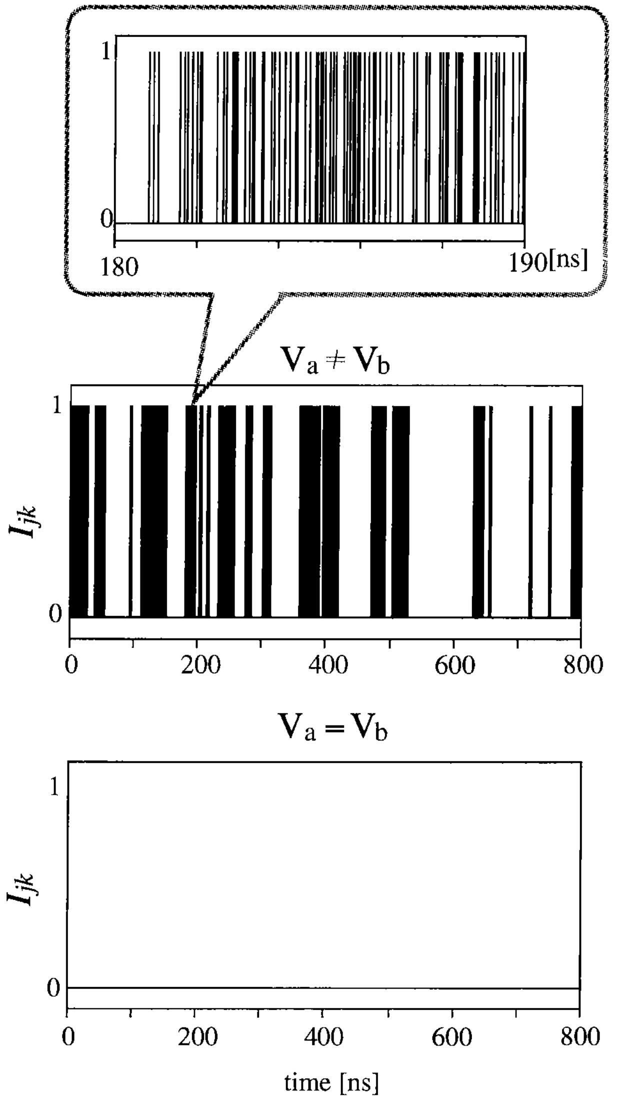

Fig. 6 Simulation results about the dependence of I_{jk} on $V_{a,b}$ in the bit-comparator.

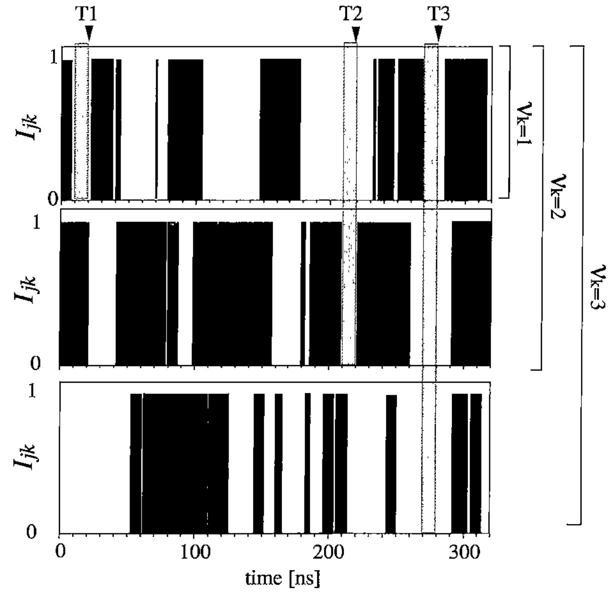

Fig. 7 Waveforms of I_{jk} and detection timing depending on ν_k.

$\zeta_{jk}, j = 1,2,3$, and detection timing depending on ν_k. Here, we assume $t_s = 10$ nsec. If only the first bit ($j = 1$) is unmatched, the first time when $V_k = 0$ is T_1. If the first and second bits ($j = 1,2$) are unmatched, the first time when $V_k = 0$ is T_2. If the first to third bits ($j = 1,2,3$) are unmatched, the first time when $V_k = 0$ is T_3. We can apparently see that $T_1 < T_2 < T_3$.

5. Discussion

5.1 XOR Circuit Using SET Devices

The bit-comparator described in Sect. 3 is a kind of XOR circuit in which the output is "0" when the two inputs are the same, and the output oscillates when the two are different. If the output is integrated as described in Sect. 3.1, XOR logic is achieved in the strict sense. Thus, we have demonstrated that XOR logic can be constructed using only an inverter and a switch with SET devices. The circuit is clearly much simpler than the conventional digital XOR circuit.

5.2 Difference between Stochastic Associative Memory and Chaotic Associative Memory

An associative memory constructed using chaotic neural networks continues to retrieve various patterns including all stored patterns non-periodically. In another chaotic associative memory, when the output becomes close to one of the stored patterns, the state is forced to jump away from that pattern rapidly by its dynamics [6]. Internal states of such memories are in chaotic itinerancy, which may be a model of associative retrieval occurring in the human brain.

The associative memory proposed in this paper stochastically outputs a similar pattern according to the order of similarity. If we feed this obtained output pattern back to the input, this memory continues to retrieve sequential patterns in which the consecutive patterns are almost the same but sometimes different. In this output sequence, very different patterns are hardly retrieved directly. However, by continuing retrieval for a longer time, patterns emerge that are far different from the starting pattern. This may be another model of associative retrieval occurring in the human brain.

6. Conclusion

We proposed a new associative memory architecture utilizing stochastic behavior in SET devices. This memory stochastically associates the pattern most similar to the input key pattern. We proposed two modes for pattern matching. In the voltage-domain matching mode, ordinary associative memory operation can be performed; in the time-domain matching mode, a purely stochastic search is carried out. We described a circuit using SET devices based on this architecture and demonstrated its basic operation with a simulation. We also proposed a new consecutive association model by feeding the output pattern back to the input. The proposed model and architecture may become a component of intelligent information processing systems close to the human brain.

Acknowledgment

The authors wish to thank Prof. Masataka Hirose for his support and encouragement and also thank Prof. Yoshihito Amemiya for his valuable advice. This work has been supported in part by Grants-in-aid for the Core Research for Evolutional Science and Technology (CREST) from Japan Science and Technology Corporation (JST).

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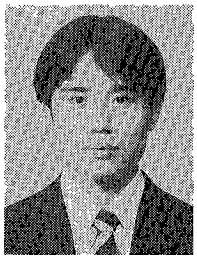

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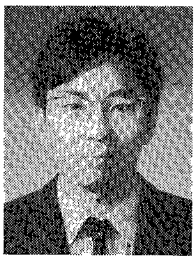

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