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Design of a Wireless Neural-Sensing LSI

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SUMMARY We propose a neural-sensing LSI with a bi-directional wireless interface, which is capable of detecting 5-channel neural signals in a living animal. The proposed sensing LSI consists of a multiplexer with 5-channels selectable from 10 channels, a chopper amplifier using a new direct-chopper-input scheme, a programmable multi-mode analog-to-digital converter (ADC), and a wireless-transmitter/receiver with BPSK modulation signals. The test-chip was implemented by mixed-signal 0.35-μm CMOS technology. We measured the test chip and confirmed basic operations of these blocks. The chopper-amplifier achieved 66-dB DC gain, bandwidth of 400 kHz, and 4-μV noise with power dissipation of 6-mW with a 3-V supply. We observed real nerve signals in a living cricket using the proposed chopper amplifier. ADC achieved 52-ksps operation with power dissipation of 0.43-mW at 3-V supply. The wireless transmitter achieved 1-Mbps data transmission at a distance of 1-m with 1.5-mW power dissipation at 3-V supply.

key words: *neural-sensing LSI, wireless communication, multi-input-channels, chopper amplifier, flicker noise, multi-mode ADC*

1. Introduction

Various neural signal sensors and recorders were developed by LSI technologies for application to physiology and neuroscience experiments and implantable clinical systems [1]–[3]. CMOS-LSI technologies implement a high-density and highly functional system. However, a MOSFET has large flicker noise and large deviation of device parameters. General CMOS operational-amplifiers (OPA) are not applicable to enhance weak (a few ten of μV) neural signals. However, the chopper-stabilization technique developed to reduce flicker noise still has many disadvantages. For sensing of neural signals, a buffer amplifier, such as a source follower, is required for probe impedance conversion. Noise is not reduced because it is applied before chopper modulation. For multi-channel sensing systems, multi-amplifiers that consume power and chip area are required.

Intelligent neural signal sensor LSI must transmit sensing data and receive system control commands, such as channel select, amplifier gain, and ADC operation mode. Recently, a neural stimulation system with an inductive coupled interface was developed with an 8.3-kbps data transfer rate using a 4-MHz carrier frequency [4]. The bit rate is not sufficient for transmitting time-division multiplexed multi-channel data. Furthermore, the transmission distance is limited to only a few cm.

We propose an architecture and circuits for a neural sensing system to resolve these problems. To achieve accurate and efficient neural signal sensing, we measured neural signals in a living animal and designed the specification of the sensing system. Major items in the specification are voltage gain and bandwidth of the low noise amplifier, resolution and sampling rate of the ADC, and wireless transmission data packet format. We propose a wireless transmitter/receiver (TX/RX) circuit with a data transmission rate of 1 Mbps, and a low power ADC with multi-operation modes with a resolution range of 5–10 bits and a sampling rate range of 10–50 k-sampling-per-second (ksps)/channel. We evaluated a test chip of the proposed sensing system-LSI, which was fabricated in a 0.35-μm CMOS process. This paper also describes measurement results obtained using the test chip. We confirmed that the proposed direct-chopper-input amplifier could detect real weak nerve signals in a living cricket. Analog-to-digital conversion of multiplexed neural signals and wireless data transmission were demonstrated.

2. System Architecture

We have already implemented in a neural signal measurement circuit of a fish cerebellum using discrete JFET-OPAs and an existing ADC. The system requirement for neural signal sensing is the ability to compare detected neural signal waveforms with memorized reference waveforms, and to identify the type of neural activity. Figure 1 shows the neural

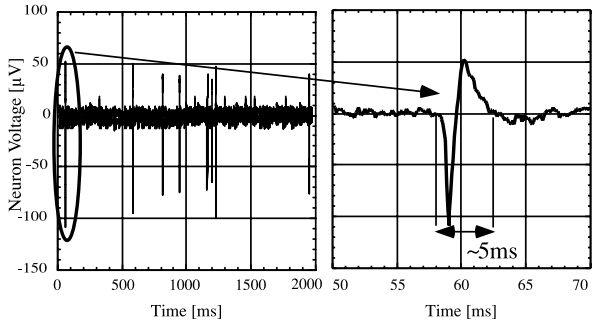

Fig. 1 The neural waveform of a fish cerebellum measured by discrete OPAs and existing 8-bit ADC.

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waveform of a fish cerebellum observed using the measurement circuit. The neural signal is weak (~100 μV), slow (~5 kHz), and has a firing rate of a few times per second. The pulse width of the signal is about 5 ms. Thus, a neural sensing-system requires an amplifier with DC-gain of about 80 dB and an ADC, which operates at more than 10-ksps and 8-bit accuracy to analyze the measured waveform on a PC. Moreover, when measuring the neural signal in a living fish, the sensing system should transmit measured data from within water. We confirmed the electromagnetic wave propagation characteristics in water using a 2-cm-ϕ loop antenna, an acrylic tank measuring 0.9 m in length, and 0.5 m in width and height. A transmitter operating at a frequency of 100 MHz achieved a data transmission rate of 1 Mbps. Thus, we determined the carrier frequency of the sensing-system to be 100 MHz.

We propose a wireless multi-channel neural sensing system implemented as a one-chip LSI, consisting of a 10-ch probe, a multiplexer/amplifier (MUX/AMP) block, a 10-bit ADC block, and a wireless TX/RX block including a voltage-controlled oscillator (VCO). The block diagram of the proposed system is shown in Fig. 2. The 10-ch probe has 10-tungsten-needles in a local area of 2-mm-ϕ. It is possible that the system observes the behavior of various neurons. As it is possible that not all needles will detect a significant signal, the MUX/AMP block chooses any 5-channels from the 10-ch probe by a channel selection command.

The MUX/AMP block multiplexes the signals of the chosen 5 channels at a pulse width of less than 20 μs, because it is necessary for the ADC block to digitize every signal of the chosen channel at more than 10 ksps. The MUX/AMP block is supplied with a 52-kHz clock signal from the VCO, and thus the pulse width is about 19.2 μs and ADC sampling rate is 52 ksps. Moreover, MUX/AMP block requires a DC-gain of about 80 dB and a reduction of flicker noise and voltage offset because the neural signals are typically weak (a few ten of μV) and slow (a few kHz).

The ADC block has 10-bit resolution to achieve 8-bit accuracy. The ADC block has 3 operation modes to achieve effective measurements as follows: the ADC digitizes (1) neuron firing rate at 5-bit resolution, 10.4 ksps per channel in low-resolution mode, (2) 5 waveforms at 10-bit, 10.4 ksps per channel in high-resolution mode, and (3) waveform at 10-bit, 52 ksps per channel in high-speed sampling mode.

The TX/RX block consists of a transmitter, receiver, and VCO. The VCO, which is implemented by off-chip inductors, supplies a carrier frequency of TX/RX block and system clock at an operation frequency of 100 MHz. The TX transmits an ADC output data and system status data to an external receiver. The RX receives the sensing-LSI control data, such as the probe selection command and resolution control command, from the external transmitter. The external transmitter/receiver is implemented using commercially produced devices, including a low-noise amplifier, power amplifier, modulator, and demodulator. We designed the external transmitter/receiver to be able to vary transmission power to achieve a simplified system. Thus, the RX is not equipped with a variable gain-control amplifier. The system does not take into consideration interference or disturbance from other frequency channels because the actual experiments are performed using an electromagnetic shield.

The data forms of transmission and reception are shown in Fig. 3. The transmission data are transmitted to the external receiver at 520 kbps due to the operation of the 10-bit ADC at 52 ksps. We determined that the length of the transmission packet, which consists of a header and

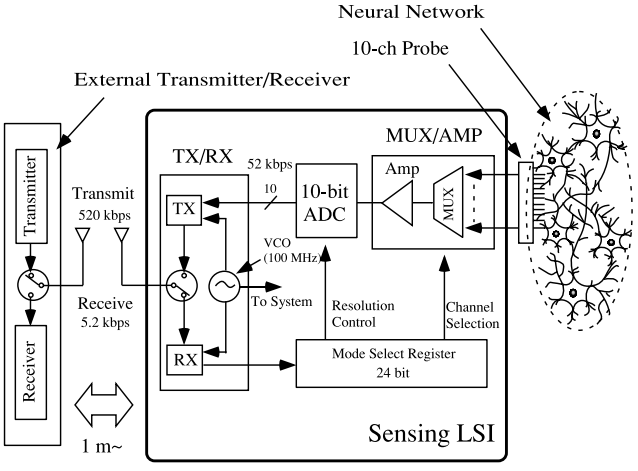

Fig. 2 Proposed wireless neural-sensing system.

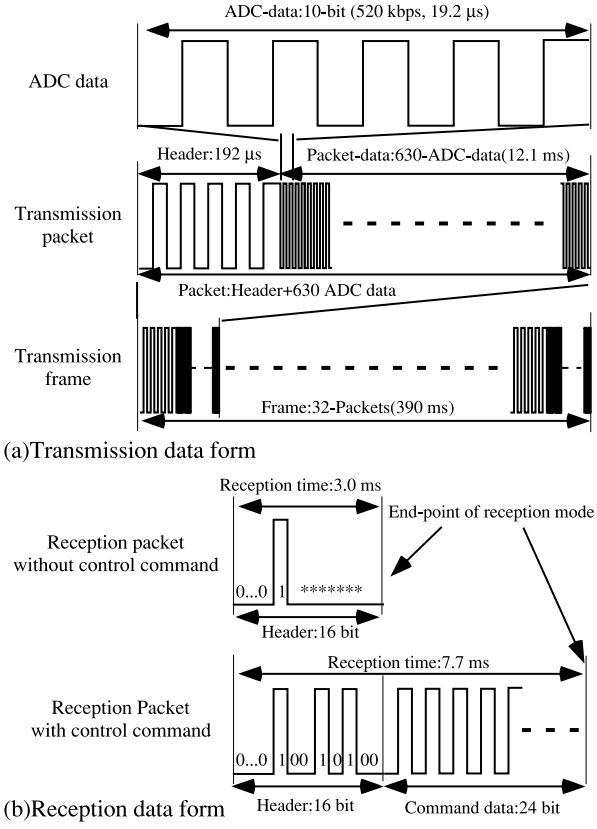

Fig. 3 Proposed data formats of (a) transmission and (b) reception.

630 ADC data, is more than double the neural signal pulse width. The header is required to synchronize with the external transmitter/receiver. A transmission frame consists of 32 transmission packets and the length of the frame is about 390 ms.

After the TX transmits the transmission frame, the RX accepts the header of the reception packet, consisting of 16-bit data, from the external transmitter for about 3 ms. When the RX receives the header, which includes a control command, the RX also receives 24-bit command data at 5.2 kbps. In the case of the header without the control command, the RX finishes receiving the command data, and the TX transmits the transmission frame again.

3. Circuit Design

3.1 TX/RX Block

The TX/RX block diagram is shown in Fig. 4. The block consists of the VCO, binary phase shift keying (BPSK) mixer (up and down), Output Buffer, amplifiers, LPF, and logic circuits. The logic circuits include a modified frequency modulation (MFM) encoder, header decoder, and frame counter. The MFM encoder, which is used for floppy disk format, is implemented in this block, because the MFM achieves a mark ratio of about 50% in the transmission data. The TX transmits the MFM encoded ADC-data to the external receiver using the BPSK modulation in the case of data transmission. In the case of data reception, the RX decodes the BPSK modulated RF data using a direct conversion method. When the header-decoder detects the LSI control command from the external transmitter, the frame counter block extends a reception time and the RX receives the command data.

Figure 5 shows a schematic of the transmitter circuit, which includes the VCO, the BPSK up-conversion mixer and the output buffer. The VCO is implemented with MOS varactors and external inductors. BPSK modulation is accomplished by switching of differential outputs of the VCO. In the case of operation at 100 MHz, the power dissipation of the VCO and the VCO buffer are 60 μW and 600 μW at a supply voltage of 3 V, respectively. The number of logic gates in the TX/RX block is about 1.2 k, and the power consumption is 0.6 mW at a supply voltage of 3 V, as confirmed by HSIM simulation.

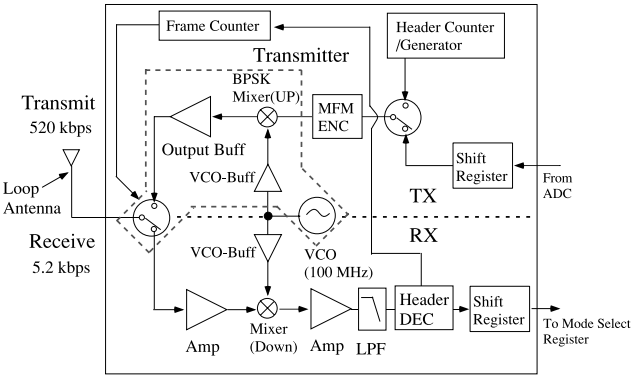

Fig. 4 TX/RX block diagram.

3.2 ADC Block

The ADC block digitizes a multiplexed and amplified neural signal for digital wireless communication. The ADC requires more than 8-bit accuracy for waveform analysis on a PC. Therefore, we designed a 10-bit resister-capacitor-hybrid charge-redistribution ADC with 3 operation modes. The ADC block is illustrated in Fig. 6. The block includes an R-31R-resister-string, coarse-and-fine capacitor array, 3-stage inverter-chopper-comparator, and a successive-approximation register (SAR). The value

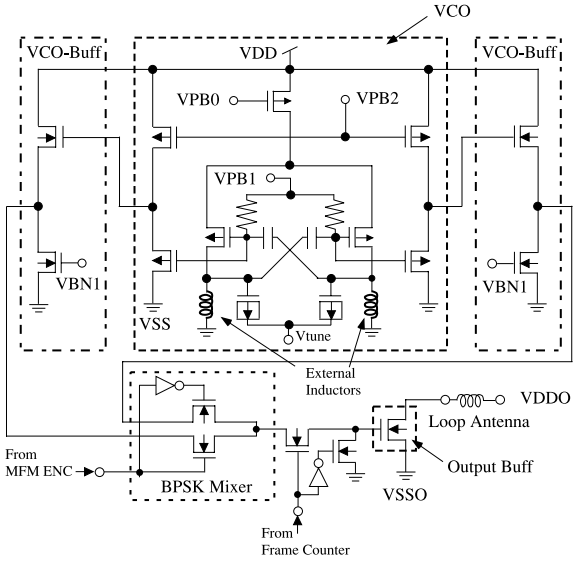

Fig. 5 Schematic of the transmitter circuit.

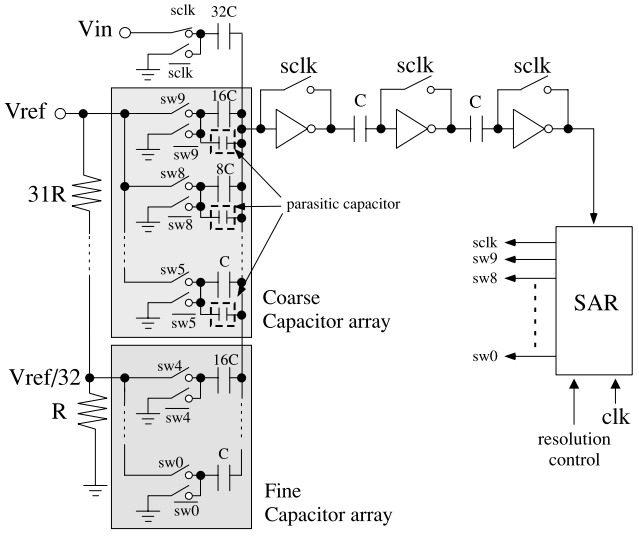

Fig. 6 Block diagram of resistor-capacitor-hybrid charge-redistributed ADC.

of the unit capacitor C is 0.7 pF. The SAR controls only a coarse capacitor array in low-resolution mode, and the ADC achieves 5-bit resolution. In the other modes, the ADC fully digitizes 5-multiplexed signal (high-resolution mode) or unmultiplexed signal (high-speed sampling mode) at 52 ksps. The comparator achieves a 100-dB DC-gain and a bandwidth of 1 MHz. R and 31R of the resistor-string are connected to a fine and coarse capacitor array, respectively. The proposed hybrid ADC minimizes the overhead clock, which consists of a sampling clock (sclk) and a reset clock of SAR. However, the ADC requires a fine capacitor array.

We simulated the ADC with extracted parasitic components. However, deviation of each component was not considered. The simulated differential and integral nonlinearities (DNL and INL) are shown in Fig. 7. The largest DNL and INL were less than 0.5 LSB and 0.4 LSB, respectively. The largest error is caused by the parasitic capacitor, located between the coarse capacitor array common node and the terminals of the capacitors. Thus, the degradation of nonlinearities is improved, increasing the value of the unit capacitor. The proposed ADC achieved 52 ksps operation at a clock of 600 kHz, and a power dissipation of 0.43 mW at a supply voltage of 3 V.

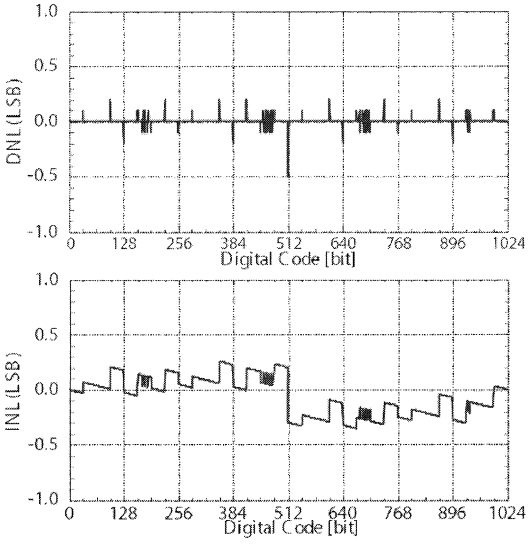

Fig. 7 Simulated DNL and INL.

3.3 MUX/AMP Block

The MUX/AMP block amplifies the difference between a detected voltage near the focused neuron and a reference voltage (Vref) defines the voltage of the cell liquid far from the observed neuron. The amplifier of the MUX/AMP block requires 80-dB DC-gain, 10-μV in-band noise, and 10-μV offset voltage to amplify neural signals. To implement such a low noise amplifier, a chopper technique is adopted [5]. As the output resistance of the needle inserted into the brain is as high as a few MΩ, the MUX/AMP block requires an input impedance higher than the output resistance. However, the input impedance of the chopper amplifier is low because of charge/discharge of chopper stray capacitance operated at a high modulation frequency.

To solve this problem, we proposed a direct-chopper-input scheme [6], as shown in Fig. 8. An equivalent circuit of the neuron/needle interface is also shown in the same figure. The equivalent neuron circuit consists of a nucleus and a cell membrane. The nucleus outputs a 100-mVpp voltage pulse at a few kHz and the membrane is represented as having resistance of 3 MΩ and capacitance of 3 pF [7]. The pulse is attenuated to about 100 μV in *in-vitro* testing because of the attenuation ratio of resistance of the cell liquid versus that of the membrane. Due to the polarization charge, the tungsten probe also has liquid/needle interface impedance, which consists of 10-MΩ and 10-kΩ resistance and 1.7-nF capacitance.

We simulated applicability of the direct-chopper-input scheme to a practical neural system environment using an equivalent circuit as shown in Fig. 8. Simulation results showed that the voltage transfer (Vout/Vin) is 0.96 at a chop-

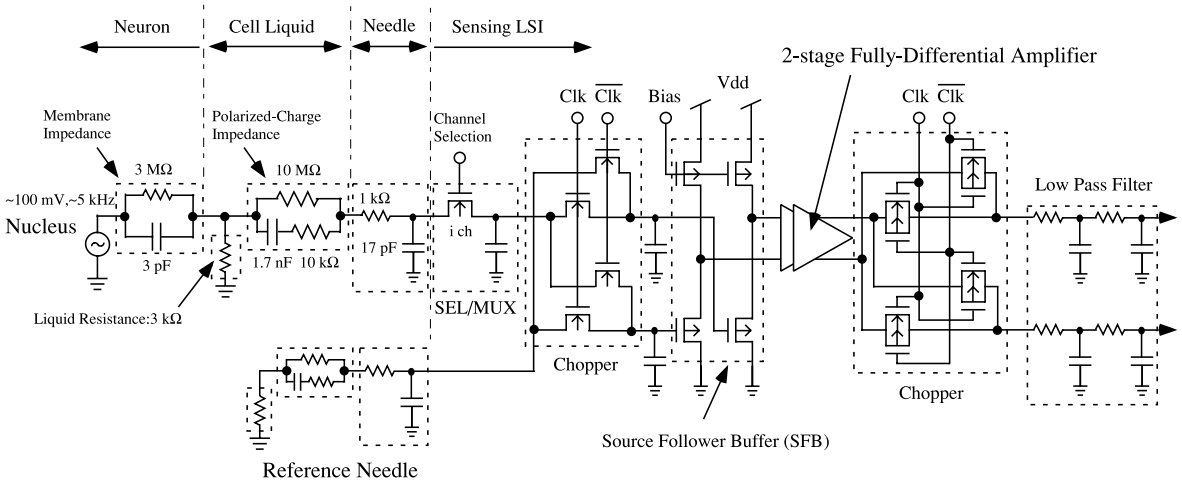

Fig. 8 Proposed direct-chopper-input scheme and neuron probing equivalent circuit.

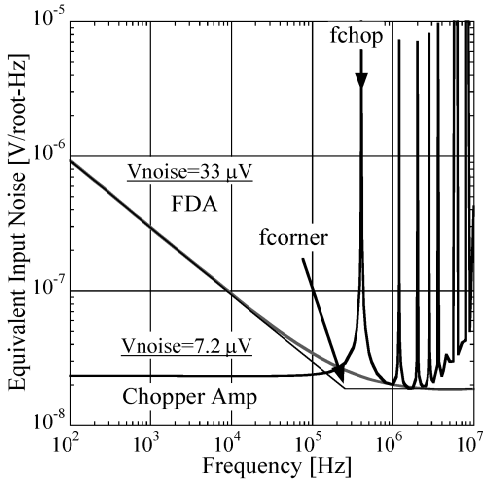

Fig. 9 Simulated noise spectral density.

per clock of 400 kHz because the large probe capacitance (Cp = 17 pF) operates as a charge reservoir

The MUX/AMP block, consisting of a selector/multiplexer (SEL/MUX), an input chopper for modulation, source follower buffers, two fully-differential amplifiers (FDAs) with capacitor feedback, an output chopper for demodulation, and a low pass filter, is also shown in Fig. 8. The FDA was designed to have about 40-MHz unity-gain bandwidth, and 70-dB open-loop-gain. The capacitor feedback amplifier has 38-dB DC-gain and a cut-off frequency of 500 kHz. The simulated noise spectral density of the chopper amplifier is shown in Fig. 10, in comparison with the FDA. Equivalent input noise of the FDA is 33 μV and the noise corner frequency is 250 kHz, as shown in Fig. 9. The chopper frequency is 400 kHz, which is higher than the noise corner frequency. The overall chopper amplifier has 76-dB DC-gain and a cut-off frequency of 400 kHz. The equivalent input noise is reduced to 23 nV/root-Hz. Total in-band noise (~100 kHz) is reduced to 7.2 μV.

4. Experimental Results

The proposed sensing system was designed and fabricated with a 0.35-μm double-poly triple-metal CMOS technology. The test chip included a MUX/AMP block, an ADC block, and a TX block, as shown in Fig. 10, and the chip area was 25 mm^2 (= 4.9 × 4.9 mm^2).

The output spectrum of the TX block with BPSK modulation is shown in Fig. 11. The VCO with an output buffer had an oscillator frequency of 110.6 MHz, and the BPSK modulation frequency was 500 kHz. We confirmed that the output spectra consisted of oscillator frequency and harmonic components of the BPSK modulation frequency. The power dissipation of the VCO and the output buffer were 0.6 mW and 0.9 mW, respectively, at a supply voltage of 3 V. The received data of the external receiver is shown in Fig. 12, when the TX block output the BPSK modulation data from a 2-cm-ϕ loop-antenna. The test chip was kept

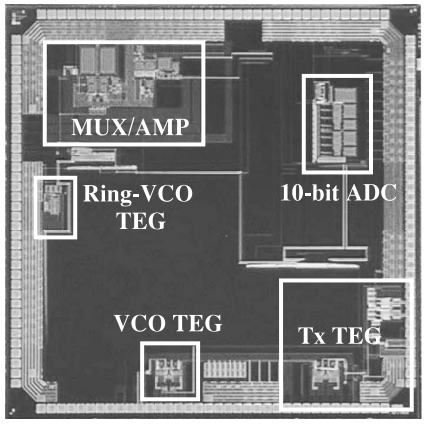

Fig. 10 Test chip of the proposed neural sensing system.

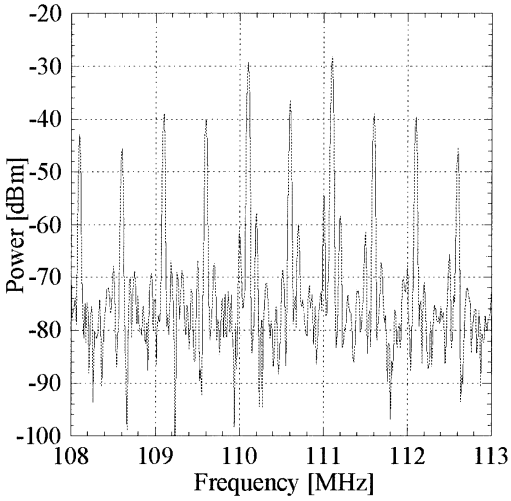

Fig. 11 Output spectrum of TX with BPSK modulation.

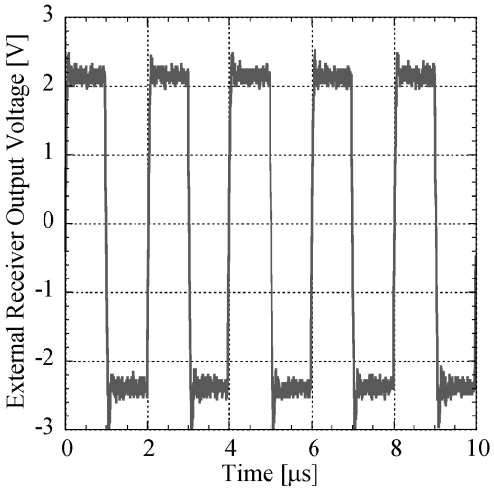

Fig. 12 Output waveform demodulated by the external receiver.

at a distance of 1 m from the external transmitter/receiver with a 3-m dipole antenna. The external receiver had a minimum reception power of −107.8 dBm. We confirmed that

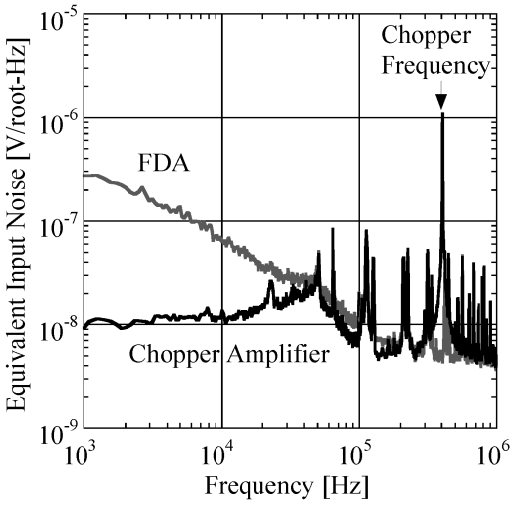

Fig. 13 Measured noise spectrum density.

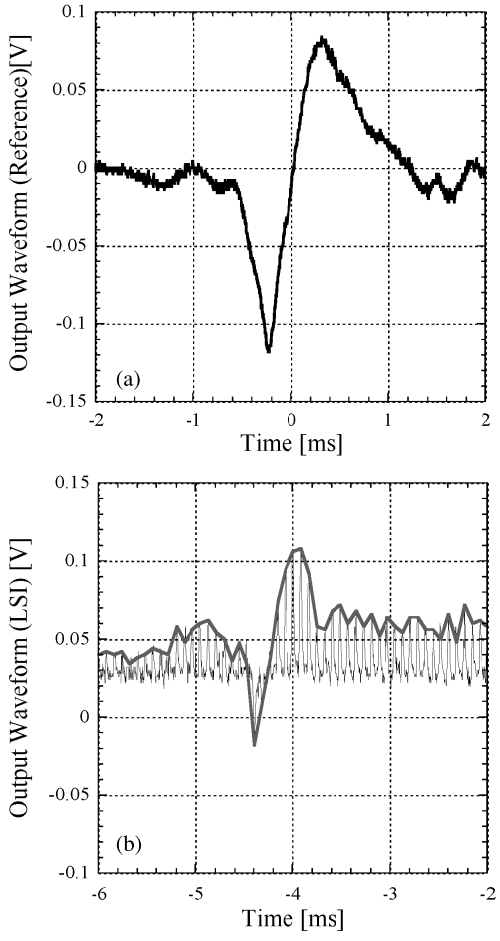

Fig. 14 (a) Measured neural waveform using a measurement circuit implemented by discrete-OPAs, and (b) measured neural waveform using the proposed MUX/AMP.

the TX block enabled a data transmission rate of 1 Mbps using BPSK modulation.

The measured noise spectrum density of chopper amplifier and FDA are shown in Fig. 13. The chopper frequency was 400 kHz, and the input terminals were connected to the ground of an evaluation board. The FDA had a corner frequency of 250 kHz and a total in-band noise of 23.0 μV (~100 kHz). The chopper amplifier achieved the equivalent input noise of 10-nV/root-Hz and the total in-band noise of 4.0 μV. Figure 13 shows that the chopper amplifier reduced low-frequency noise of FDA. A strong peak is observed at the chopper frequency due to modulation of flicker noise. The chopper amplifier achieved a 66-dB DC-gain and cut-off frequency of 400 kHz. The measured power dissipation of the MUX/AMP at a supply voltage of 3 V was 6.0 mW.

We measured neural signals of a cricket leg nerve fascicle to evaluate the proposed MUX/AMP. Figure 14 shows (a) a measured waveform using a measurement circuit implemented by discrete-OPAs, and (b) a measured waveform using the proposed MUX/AMP. Initially, we inserted 250-μ-ϕ stainless needles into the leg of the cricket. Next, the measurement circuit was used to observe the neural signal as a reference using the inserted needles. Finally, the MUX/AMP measured the neural signal using the same needles. The measurement circuit was equipped with a 66-dB DC-gain and band-pass-filter with bandwidth of 20 Hz to 5 kHz. The input channel of the MUX/AMP was connected to the needle adjacent to the nerve, and the other 4 channels were connected to the reference probe. The proposed direct-chopper-input scheme achieved detection of the neural signal.

5. Conclusion

We proposed a neural-sensing LSI with a bi-directional wireless interface, which consisted of a multiplexer, a chopper amplifier, a programmable multi-mode ADC, and a wireless transmitter/receiver. The proposed LSI was shown to be able to detect 5-channel neural signals in a living animal. We confirmed basic operations of these blocks using a test chip, which was implemented with a mixed-signal 0.35-μm CMOS technology. The chopper-amplifier showed 66-dB DC gain and 4-μV in-band noise, and observed real nerve signals in a living cricket. Power dissipation of the chopper amplifier was 6-mW at 3-V supply. The ADC achieved 52-ksps operation at a clock of 600 kHz. The wireless transmitter accomplished a data transmission rate of 1 Mbps at a distance of 1 m. The power dissipation of ADC and transmitter were 0.43 mW and 1.5 mW, respectively, at a supply voltage of 3 V.

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