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A 2.7 Gcps and 7-Multiplexing CDMA Serial Communication Chip Using Two-Step Synchronization Technique

Mitsuru SHIOZAKI[†a)], ***Member***, **Toru MUKAI**[†], ***Nonmember***, **Masahiro ONO**[†], ***Student Member***, **Mamoru SASAKI**[†], ***and*** **Atsushi IWATA**[†], ***Members***

SUMMARY Intelligent robot control systems based on multiprocessors, sensors, and actuators require a flexible network for communicating various types of real-time data (e.g. sensing data, interrupt signals). Furthermore, serial data transfer implemented using a few wiring lines is also required. Therefore, a CDMA serial communication interface with a new two-step synchronization technique is proposed to counter these problems. The transmitter and receiver fabricated by 0.25 μm digital CMOS technology achieve 2.7 Gcps (gigachips per second) and can multiplex 7 communication channels.

key words: *CDMA, robot, multiplex, synchronization technique*

1. Introduction

Advanced robot control systems are composed of several subsystems of multiprocessors, sensors, and actuators, and they require several new technologies and highly integrated components. The first requirement is to implement a real-time and flexible communication network in order to satisfy the restriction on the sampling time of sensing and control and to transfer varying amounts of real-time data, e.g., large amounts of image data from sensors and small amounts of command data to the actuators. If a large number of wiring lines was required to connect each subsystem, they will restrict smooth and high speed movements of robot arms and hands. Therefore, the robot control network should be implemented with a small number of wiring lines.

It is difficult for TDMA (Time-Division Multiple Access) to communicate varying amounts of real-time data within a restricted time frame because the data are transmitted in packets or frames of a fixed size [1], [2]. Furthermore, dynamic variation of communication channels and channel bandwidth is difficult because its control overhead is heavy and a flexible network can only be obtained at the cost of transmission efficiency.

We propose a communication scheme appropriate for the robot control system with CDMA (Code-Division Multiple Access) serial communication being the key idea. The CDMA technique enables multiplexing and transfers of data with several virtual paths using a single wire. Various types of data can be transmitted independently through the virtual paths.

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[†]The authors are with the Graduate School of Advanced Sciences of Matter, Hiroshima University, Higashihiroshima-shi, 739-8530 Japan.
a) E-mail: shiozaki@dsl.hiroshima-u.ac.jp

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Several researches have been reported wherein the CDMA scheme has been implemented with wired communication [3], [4]. The CDMA system with a bus configuration has been implemented in [3]. The bus configuration was implemented using multiple connections of transmitters with switched-capacitor charge pump circuits to a single wire line. The input and output impedances are drastically changed when the circuit switches. This mismatch that occurs because a transmitted waveform is distorted by the influence of multiplex reflection results in a low data transfer rate, i.e., less than approximately 100 Mbps. In addition, it stets sufficient time to charge and stabilize all nodes of the transmitter. The CDMA scheme has also been applied in point-to-point serial links, and a communication chip for this purpose has been developed [4]. Although a high data transfer rate of 2.7 Gcps has been achieved, the number of multiplexed channels is limited to two. In order to increase the number of CDMA channels, a new synchronization technique between the transmitter (TX) and receiver (RX) is required. CDMA systems transmit multiplexed multivalued signals with several amplitude steps. As the number of amplitude steps increases, the size of each step decreases. Therefore, the synchronization technique used for time-multiplexed serial links is not applicable to the CDMA serial link because it only detects the rising edges of the received signals.

This paper proposes a two-step synchronization technique for highly multiplexed CDMA signals. The synchronization, which includes code and chip synchronization, is developed by utilizing the specified short code that does not process optimal properties for synchronization [5], [6]. The code synchronization can adjust the starting time of the decoding operation of the received sequence, and it corresponds with the initial acquisition process in a conventional CDMA system. The chip synchronization implemented with a DLL (Delay Lock Loop) is capable of adjusting the timing of each pulse. The two-step synchronization technique has been applied to the CDMA system in a point-to-point link, which can operate as a bus. The test chip with a transmitter and receiver for the CDMA serial communication system was designed and fabricated by 0.25 μm digital CMOS technology. The proposed CDMA system achieved multi-Gcps P-to-P data transfer performance.

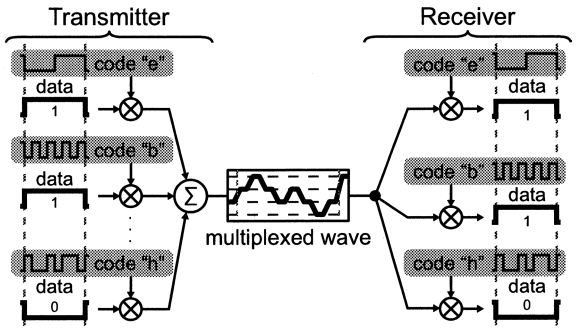

Fig. 1 Block diagram of the CDMA system.

2. CDMA (Code-Division Multiple Access)

A conceptual block diagram of the CDMA communication system is shown in Fig. 1. In the transmitter, data are encoded by the spread code set and each encoded signal is multiplexed by summation and sent out through a transmission line. In the receiver, the transmitted data can be reconstructed by decoding the received signal. The decoding is processed by a correlation operation between the received signal and the same code that was used for encoding in the transmitter.

2.1 Spread Code

For the spread codes in CDMA systems, two types of correlation properties—a cross-correlation property and an autocorrelation property—are required.

The cross-correlation property indicates the interferences (orthogonalities) among the spread codes. If the cross-correlation function described by Eq. (1) is zero among all codes, the mutual interferences are very small and the communication system has a low BER (Bit Error Rate).

$$r_{ij} = \sum_{n=1}^{N} Y_i(n) \cdot Y_j(n) \tag{1}$$

where $Y_i(n)$ and $Y_j(n)$ represent nth codes. The autocorrelation property indicates similarity according to the phase shift of a code, and it is a convenient property for synchronization. The code used for synchronization should have a high autocorrelation value, as shown in Eq. (2), only when the time shift equals zero.

$$r_i(k) = \sum_{n=1}^{N} Y_i(n) \cdot Y_i(n+k) \tag{2}$$

where $Y_i(n)$ is an nth code and $Y_i(n+k)$ is an $n+k$th code. It is difficult to select the best codes that have these two properties in wired CDMA communication because the codes are short as compared to those in radio communication and the types of codes available for selection are limited. M-sequence has a good autocorrelation property; however cross-correlation is not zero. Therefore, mutual interferences among codes are large. In Walsh codes, which are an orthogonal set of codes, any cross-correlation among the codes is zero. Thus, mutual interferences among the codes are very small. However, if the synchronization is incomplete during the correlation operation, the interferences among the codes are large, further, in terms of autocorrelation, the codes have an inconvenient property for synchronization.

Hence, we develop a synchronization method using the Walsh codes with low autocorrelation and explain the method in the next section. Table 1 lists the Walsh codes of length 8, which are employed as spread codes.

Table 1 The Walsh code of length 8.

Name	Code							
"a"	+1	+1	+1	+1	+1	+1	+1	+1
"b"	−1	+1	−1	+1	−1	+1	−1	+1
"c"	−1	−1	+1	+1	−1	−1	+1	+1
"d"	−1	+1	+1	−1	−1	+1	+1	−1
"e"	−1	−1	−1	−1	+1	+1	+1	+1
"f"	−1	+1	−1	+1	+1	−1	+1	−1
"g"	−1	−1	+1	+1	+1	+1	−1	−1
"h"	−1	+1	+1	−1	+1	−1	−1	+1

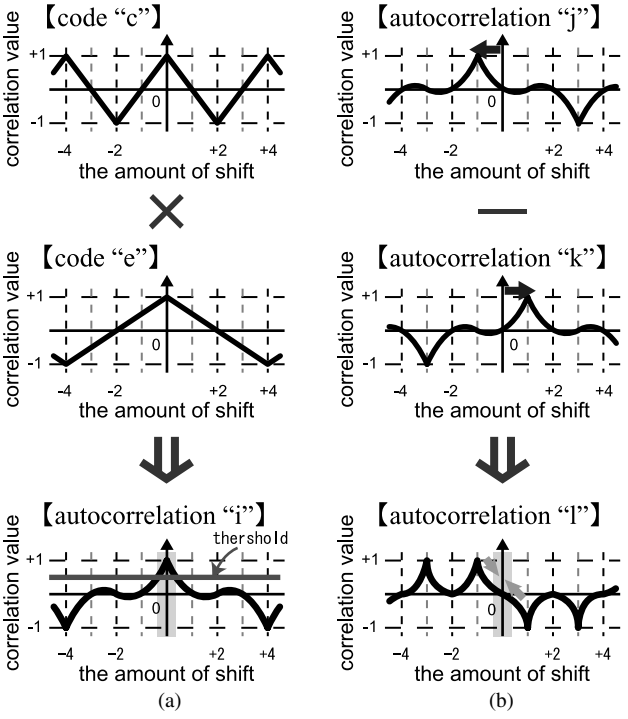

Fig. 2 Correlation function used for the synchronization. (a) The autocorrelation function "i" is used for code synchronization. (b) The autocorrelation function "l" is used for chip synchronization.

2.2 Synchronization Method

Let us consider a composition of the codes, as shown in Fig. 2(a), in order to introduce a convenient property for synchronization in autocorrelation of Walsh codes. In the autocorrelation function "i" of the composite code obtained by multiplying the codes "c" and "e," the maximum positive

value is obtained only if the shift becomes zero, and a sharp curve is observed around the maximum value. This property is very convenient for synchronization. In fact, the synchronization of the correlation operation, which is termed code synchronization, can be accomplished by determining the position at which the correlation value becomes the maximum while shifting the starting position of the correlation operation on the received sequence.

After the code synchronization, the pulse timing should also be adjusted and locked by using a DLL with a delay discriminator. This process is termed chip synchronization. Let us consider two autocorrelation functions "j" and "k," as shown in Fig. 2(b). They are obtained by shifting the autocorrelation function "i" to the left and right, respectively. The subtraction of "k" from "j" yields zero at the position where the shift equals zero. In addition, the value of subtraction moves from positive to negative around zero. Thus, by using the result of subtraction as the detected function to lock the DLL, the pulse timing can be adjusted and locked, and chip synchronization can be accomplished.

Even if positive/negative reversals of both "c" and "e" are carried out, the autocorrelation function "i" and "l" are invariable and can be used for synchronization. In order to satisfy this condition, the codes "c" and "e" should encode the same bit data. Therefore, the maximum number of multiplexed channels decreases from 8 to 7.

3. Circuit Implementation

3.1 Transmitter

Figure 3 shows a block diagram of the transmitter. Each input data is encoded in the CDMA coder. The CML (Current Mode Logic) driver outputs the multiplexed wave, as shown in Fig. 4(a). In the transmitter, the key to achieving a high speed lies in the CDMA coder. In particular, the buffer MUX is operated using the multiphase clocks given by a ring oscillator. Figure 4(b) shows the buffer MUX and the encoder in the CDMA coder. Each encoder circuit encodes a single bit using one of the 8 spread codes. The encoding is carried out by the logical EXOR operation between a data bit and the spread codes. The buffer MUXs control the CML driver. Each encoded result is inputted into the NMOS of the buffer MUX, and the multiphase clocks are inputted into other NMOSs. When the multiphase clocks turn on the two NMOSs, the buffer MUXs control the CML driver on the basis of the encoded results. In addition, since two clocks are used in the encoder, the buffer MUX can be controlled by time-sharing.

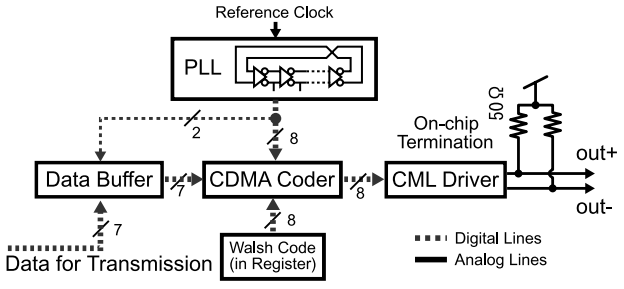

Fig. 3 Block diagram of the transmitter.

Figure 5 shows the simulation results of the CDMA coder. When the clocks "ck0" and "ck5" are high, the output encoded by the first code "b[0]" is low and the output from the buffer MUXs becomes high. Next, since both the clocks "ck1" and "ck6" become high and the output encoded by the second code "b[1]" is also high, the buffer MUX output becomes low. By repeating this operation, the buffer MUXs output signals encoded by the spread codes. Finally, the CML driver outputs the multiplexed signal by performing a voltage addition of the 8 encoded signals.

3.2 Receiver

Figure 6 shows a block diagram of the receiver circuit. The received differentialsignal is deinterleaved using wave sam-

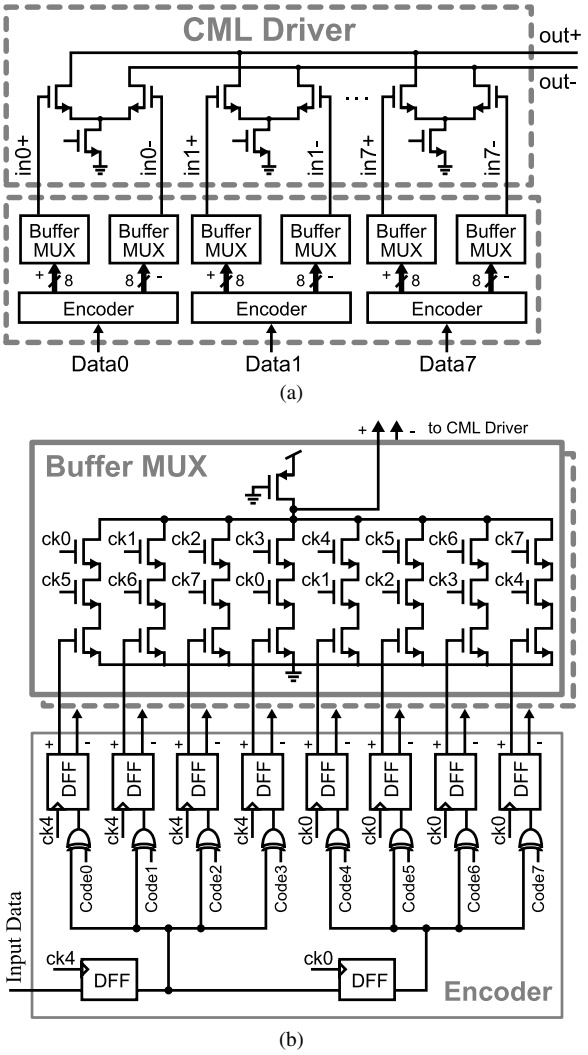

Fig. 4 The CML driver and the CDMA coder. (a) The CML driver circuit and the block diagram of the CDMA coder. (b) The circuits of the buffer MUX and the encoder in the CDMA coder.

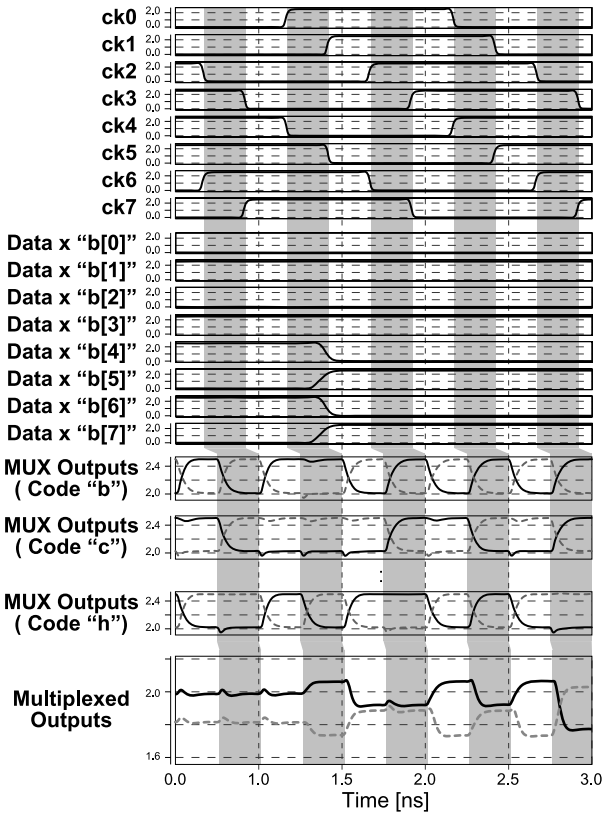

Fig. 5 Simulated waveforms of the CDMA coder.

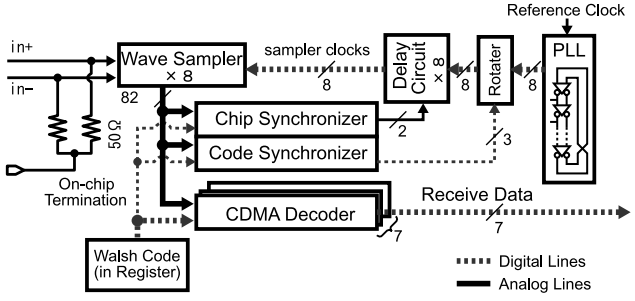

Fig. 6 Block diagram of the receiver.

plers at the two inputs that are internally terminated by 50 Ω. The number of wave samplers is equal to the length of the spread codes. The multiple clocks control the deinterleaved timing and are given by the ring oscillator although the MUX and voltage-controlled delay circuits exist between the wave samplers and the ring oscillator. The MUX and the voltage-controlled delay circuits are required for synchronization and their functions are explained in the following section.

3.2.1 Wave Sampler

The wave sampler, which aligns the phase difference of the 8 interleaved sampling waves, is composed of 3 stages of sampler blocks, as shown in Fig. 7. Figure 8 shows the timing chart of the sampling operation in the wave sampler.

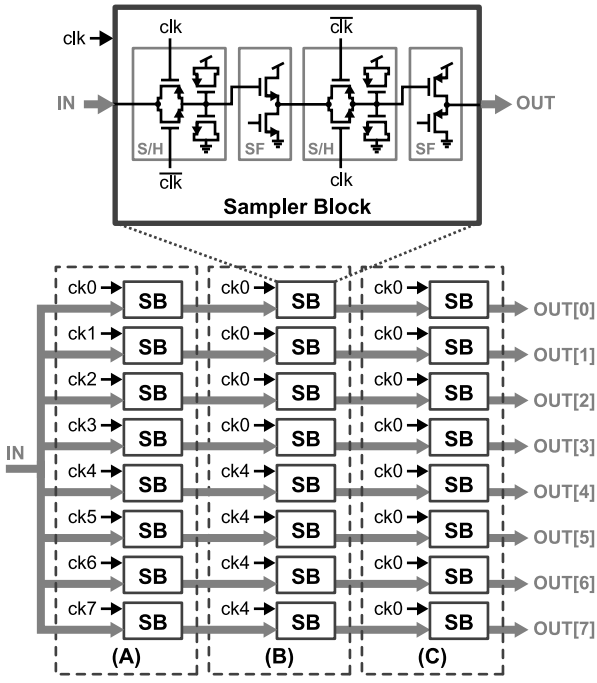

Fig. 7 Block diagram of the wave sampler.

The first set of sampler blocks (A) samples the multiplexed waves of a particular code length. The second set of sampler blocks (B) limits the phase to two groups since it is difficult to align all the phase differences. Finally, the third set of sampler blocks (C) aligns all the phase differences. Each sampler block consists of two S/H (sample and hold) circuits and source-follower buffers that are placed between the two S/H circuits. Since the two S/H circuits are in a master-slave conformation, both sampling and holding can be carried out simultaneously. In addition, since the wave sampler aligns the phase differences and lowers the operating frequency, it is possible to simplify adder circuits, explained in the next subsection.

3.2.2 CDMA Decoder

The decoder consists of 2×2 crossbar switches, a multi-input adder based on differential pairs, and a comparator, as shown in Fig. 9. The number of the crossbar switches and the inputs of the adder is equal to the length of the codes. The correlation operation is conducted on the multi-input adder by switching the crossbar in accordance with the code values "1" and "0." The comparator detects whether the result of correlation is positive or negative and outputs the 1-bit data as the result of the decoder.

3.2.3 Code Synchronizer

The code synchronizer consists of two correlators, a Gilbert cell, a comparator, a control unit, and a MUX, as shown in Fig. 10. The Gilbert cell (A) multiplies the two outputs of the correlators for the Walsh code "c" and "e." The re-

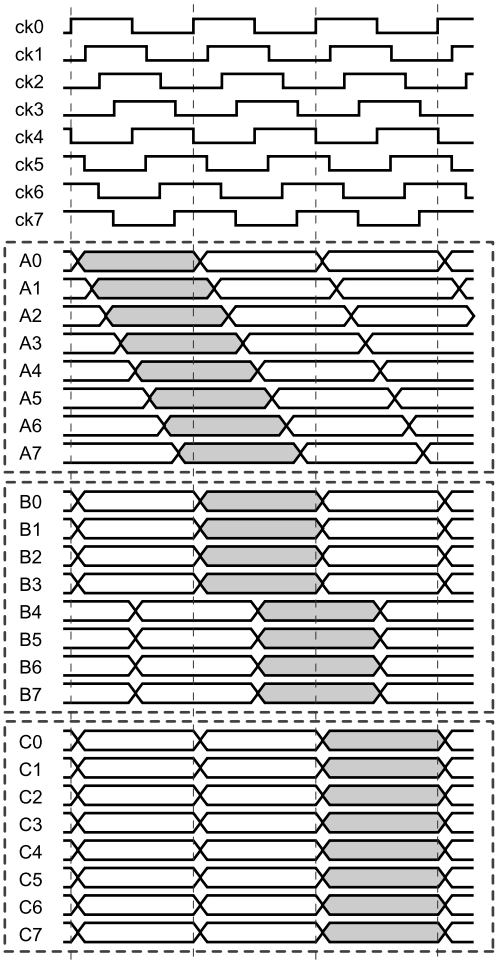

Fig. 8 Timing chart of the wave sampler.

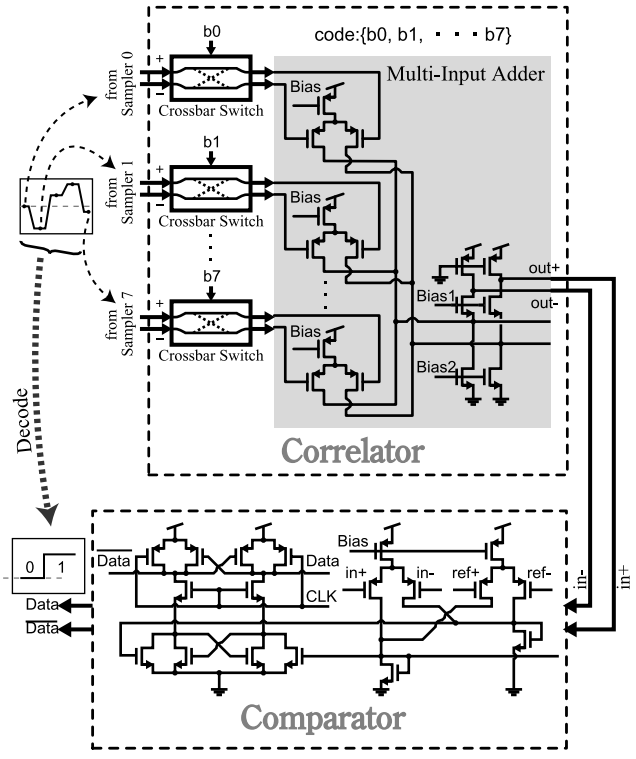

Fig. 9 Block diagram of the CDMA decoder.

sult corresponds to the autocorrelation function "i" shown in Fig. 2(a) and is compared by the comparator with a threshold. The compared result is transmitted to the control unit, which is a logic circuit. If the autocorrelation function "i" does not exceed the threshold, the control unit shifts the order of the clocks from the ring oscillator for the multi-input multi-output MUX. The frequency of the ring oscillator is locked by the PLL. On the other hand, if the autocorrelation function "i" exceeds the threshold, the unit concludes that the code synchronization has been completed, and the synchronization phase proceeds to chip synchronization.

3.2.4 Chip Synchronizer

The chip synchronizer consists of four correlators, two Gilbert cells, loop filters, and delay circuits, as shown in Fig. 10. The two Gilbert cells (B) and (C) and the four correlators generate the two autocorrelation functions "j" and "k," respectively, as shown in Fig. 2(b). Since the outputs of the two Gilbert cells are differential current signals, a subtractor can be implemented with simple wiring. Thus, these blocks function as a 2-delta delay discriminator. The outputs are filtered by the loop filters and fed to the voltage-controlled delay circuits as the differential control signals Cnt+ and Cnt−. The loop is composed of wave samplers, chip synchronizer, and delay circuits and functions as a DLL. In the code synchronization phase, Cnt+ and Cnt− are fixed at constant voltages by two switches (SW1 and SW2). SW1 and SW2 are controlled by the signal CntSW.

3.3 Flexible CDMA Communication

Figure 11 shows an example of simulated output signals of the receiver. The data (1) is continuously transferred using the 3 codes "a," "b," and "c." Two data (2) and (3) share the codes "d," "e," "f" and "g." Their bandwidth can be tuned by code assignment in real-time. First, the bandwidth of the data (2) is 250 Mbps which is obtained by using the single code "d." At 50 nsec, it increases to 500 Mbps by using the two codes "d" and "e." At the same time, the bandwidth of the data (3) changes from 750 Mbps to 500 Mbps. Thus, the data bandwidth can be suitably changed in real-time, in the CDMA chip.

4. Chip Design and Fabrication

The transceiver test chip was fabricated by 0.25 μ digital CMOS technology. The supply voltage is 2.5 V and the frequency of the reference clock is 338 MHz. The ring oscillators consist of 8 stages. The transmitter and receiver operate at 2.7 Gcps. All capacitors are implemented by MOS capacitors and all resistors are also implemented using MOS transistors that operate in the triode region. Therefore, the

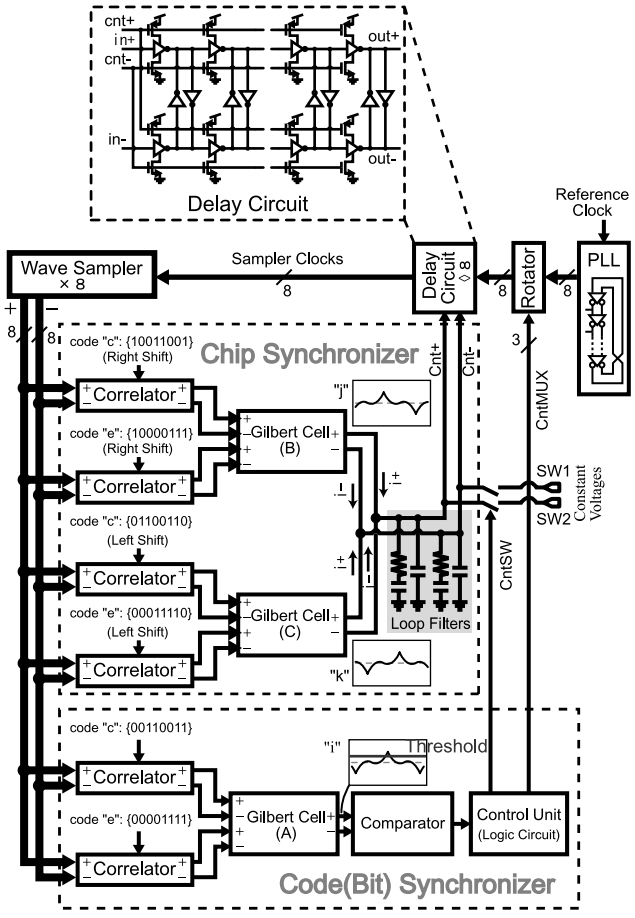

Fig. 10 Block diagram of the synchronization circuits for code and chip synchronization.

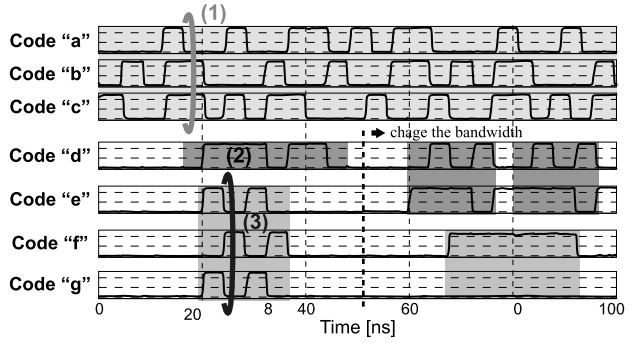

Fig. 11 Simulated waveforms of the CDMA communication.

resistance terminating at 50 Ω can be tuned by the gate voltage.

In the transmitter, the output amplitude of the differential signal for one code is set to 100 mVp-p and the multiplexed wave has a swing of 800 mVp-p because the number of multiplexed codes is 8. As mentioned in Sect. 3.1, the MUX in the CDMA coder operates at 2.7 Gcps. The other circuits operate at the 338 MHz system clock. In the receiver, the decoders operate at the 338 MHz system clock because the 2.7 Gcps signal is deinterleaved in the 8 wave samplers. Lowering the frequency facilitates easy operation of the circuit blocks.

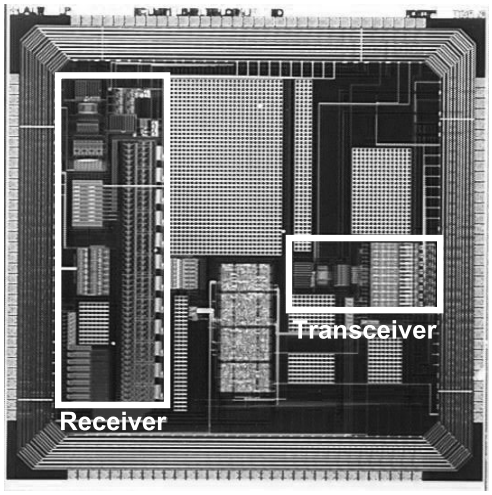

Fig. 12 Chip micrograph.

The 4.0 mm × 4.0 mm die photo of the transmitter and receiver chip is shown in Fig. 12. The chip is packaged in a 160 pin QFP plastic package. The sizes of the transmitter and receiver are 650 μm × 1300 μm and 3100 μm × 980 μm, respectively.

5. Measurement Results

5.1 Transmitter

Figure 13 shows the measurement results of the transmitter obtained at a chip rate of 2.7 Gcps. The waveforms to the left show the input data. The waveform to the right is the multiplexed CDMA signal. The measured amplitude of the multiplexed wave is 0.1 Vp-p, which is smaller than the design value (800 mV). This is because the wire length between the CML driver and MUX is approximately 0.2 mm on the chip layout. Since its time constant is large and the voltage amplitude of the driving signals is small, the MUX cannot switch the CML driver completely. The transmitter consumes 148 mW at a supply voltage of 2.5 V.

5.2 Synchronization

For the measurement of synchronizers, the multiplexed input wave was generated by an arbitrary waveform generator AWG710. Figure 14 shows the measurement results of one of the sampler clocks (multiphase clocks) after rotation. The left and right waveforms represent the sampler clock during code and chip synchronization, respectively. Since the clock is always shifted by the rotator during code synchronization, the 8 phases of the clock overlap, as shown in the figure. The extent of the phase shift equals the chip rate of 2.7 Gcps. The first sampling clock, which is measured through a source-follower buffer, is affected by crosstalk from the 338 MHz system clock. The internal clock exhibits no degradation.

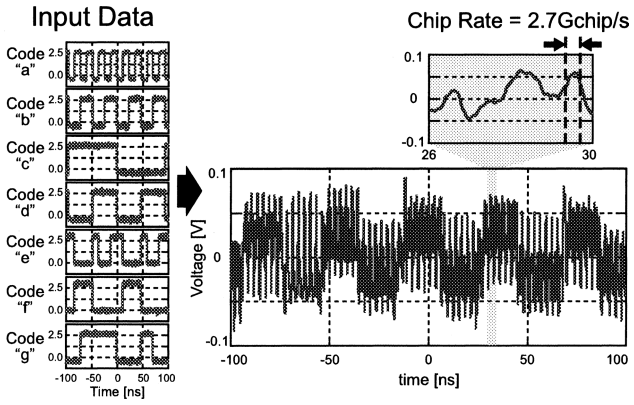

Fig. 13 Measurement results of the transmitter.

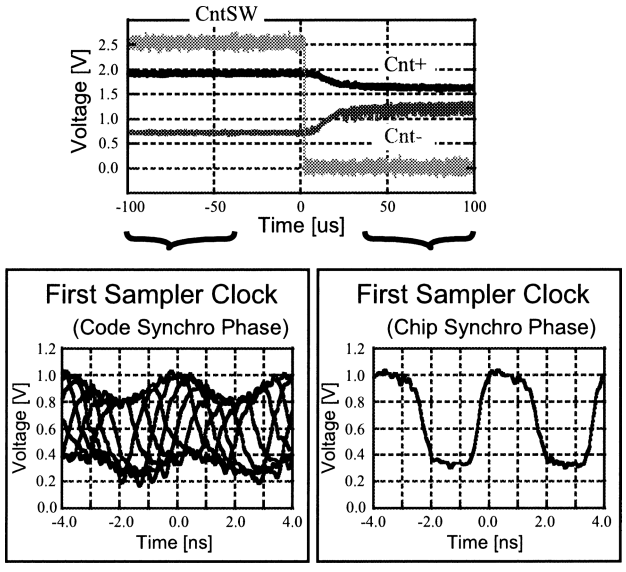

Fig. 14 Measurement results of synchronization.

On the other hand, the phase is fixed and locked during chip synchronization. The measurement results of the differential control voltages Cnt+ and Cnt− for the voltage-controlled delay circuits are also shown in Fig. 14. They are fixed at 1.9 V and 0.7 V during the code synchronization phase. CntSW is also shown in Fig. 14. It indicates the point at which the phase moves from code synchronization to chip synchronization. Cnt+ and Cnt− are adjusted and locked in the DLL during chip synchronization.

5.3 Receiver

Figure 15 shows the measurement results after decoding the multiplexed signal. The chip rate of the multiplexed wave is 2.7 Gcps. The waveforms to the left show the transmitted data from seven inputs, and the waveform in the middle is the multiplexed wave. The multiplexed wave has also been generated by an arbitrary waveform generator AWG710. Its amplitude for one code is 100 mVp-p and is used as a design value. As shown in the waveforms to the right, the receiver

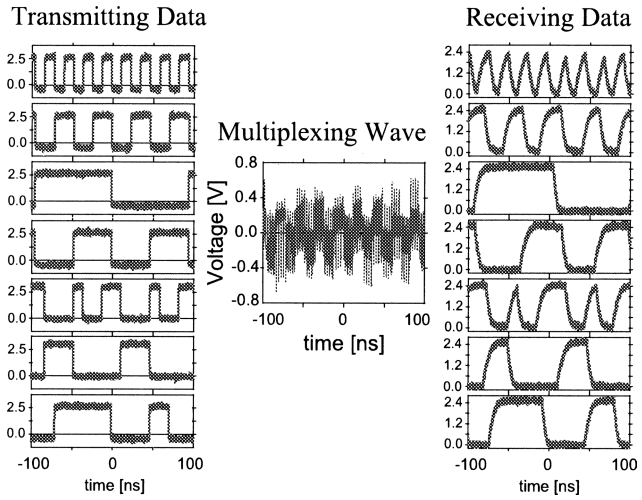

Fig. 15 Measurement results of the receiver.

has decoded the multiplexed wave by spread codes and has correctly outputted the bit sequences that are similar to those in the transmitted data. This shows that the data can be classified into a maximum of 7 groups with similar features and that it can be communicated flexibly. The receiver chip consumes 264 mW at a supply voltage of 2.5 V.

6. Conclusions

A 2.7 Gcps CDMA serial interface that multiplexes data from 7 channels, and the circuit implementations of the transmitter and receiver have been presented. The key techniques are a two-step synchronization technique for multilevel signal reception and its circuit implementation. The transceiver test chip was fabricated by 0.25 μm digital CMOS technology. It achieved a speed of 2.7 Gcps and synchronized a multiplexed signal with 7 inputs. Various real-time data of the robot system can be transferred simultaneously by the chip. In addition, since the network can be implemented with a few wire lines, which reduces the physical load on the robot, CDMA communication is suitable for the robot system. At present, we are designing a demonstration system using the CDMA serial communication chips and multiple high-speed cameras.

Acknowledgments

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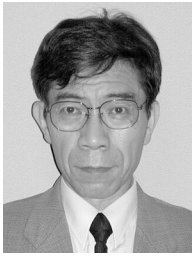
Mitsuru Shiozaki received the B.E. and M.E. degrees in electrical and electronic engineering from Ritsumeikan University in 1998 and 2000, respectively. He is currently pursuing a Ph.D. at the Department of Quantum Matter, Graduate School of Hiroshima University.

Toru Mukai received the B.E. degree in electrical engineering from Hiroshima University in 2003. He is currently pursuing a master's degree at the Department of Quantum Matter, Hiroshima University.

Masahiro Ono received the B.E. degree in electrical engineering and the M.E. degree in advanced sciences of matter from Hiroshima University in 2001 and 2003, respectively. He is currently pursuing a Ph.D. at the Department of Quantum Matter, Graduate School of Hiroshima University.

Mamoru Sasaki received the M.E. and D.E. degrees from Kumamoto University, Kumamoto, Japan, in 1988 and 1991, respectively. He is with the Advanced Science of Matter, Graduate School, Hiroshima University, where he is Associate Professor. His research interest is in analog CMOS integrated circuits and hardware implementation of wired and/or wireless communication systems.



Atsushi Iwata received the B.E., M.S. and Ph.D. degrees in electronics engineering from Nagoya University, Nagoya, Japan, in 1968, 1970 and 1994 respectively. From 1970 to 1993, he was with the Electrical Communications Laboratories, Nippon Telegraph and Telephone Corporation. He is currently a professor of Graduate School of Advanced Sciences of Matter, Hiroshima University. His research is in the field of integrated circuit design where his interests include, circuit architecture and design techniques for analog-to-digital and digital-to-analog converters, digital signal processors, ultra high-speed telecommunication IC's, and large-scale neural network implementations. He received an Outstanding Panelist Award at the 1990 International Solid-State Circuits Conference. Dr. Iwata is a member of the Institute of Electrical and Electronics Engineers.