IEICE TRANS. ELECTRON., VOL.E92–C, NO.6 JUNE 2009

PAPER Special Section on Analog Circuits and Related SoC Integration Technologies

A 2.0 Vpp Input, 0.5 V Supply Delta Amplifier with A-to-D Conversion

Yoshihiro MASUI[†a)], ***Student Member***, **Takeshi YOSHIDA**[†], ***Member***, ***and*** **Atsushi IWATA**[†], ***Fellow***

SUMMARY Recent progress in scaled CMOS technologies can enhance signal bandwidth and clock frequency of analog-digital mixed VLSIs. However, the inevitable reduction of supply voltage causes a signal voltage mismatch between a non-scaled analog chip and a scaled A-D mixed chip. To overcome this problem, we present a Delta-Amplifier (DeltAMP) which can handle larger signal amplitude than the supply voltage. DeltaAMP folds a delta signal of an input voltage within a window using a virtual ground amplifier, modulation switches and comparators. For reconstruction of the folded delta signal to the ordinal signal, Analog-Time-Digital conversion (ATD) was also proposed, in which pulse-width analog information obtained at the comparators in DeltAMP was converted to a digital signal by counting. A test chip of DeltAMP with ATD was designed and fabricated using a 90 nm CMOS technology. A 2 Vpp input voltage range and 50 μW power consumption were achieved by the measurements with a 0.5 V supply. High accuracy of 62 dB SNR was obtained at signal bandwidth of 120 kHz.

key words: *scaled CMOS technology, voltage mismatch, DeltAMP, analog-time-digital conversion (ATD)*

1. Introduction

In extremely scaled CMOS technologies, signal bandwidth and clock frequency of LSIs have been improved. However the scaled supply voltage causes voltage mismatch. Amplifiers (AMP) and Analog-to-Digital converters (ADC) made of extremely scaled CMOS technologies can not handle large voltage signals. For example, a recent sensor system requires a combination of a non-scaled analog chip with a high bias voltage, and a scaled CMOS chip for digital signal processing [1], [2]. In addition, high voltage drivers are integrated into the VLSI chip for MEMS application with the development of SOC technology [3], [4]. The interface circuits from low voltage to high voltage and high voltage to low voltage are important in the scaled CMOS technologies [5].

The purpose of this study is the development of the interface circuit from high voltage to low voltage. In general, Signal-to-Noise ratio (SNR) was reduced by using an attenuator as shown in Fig. 1. We present a Delta-Amplifier (DeltAMP) which has an interface function applicable to voltage mismatch situations. The DeltAMP can accept large signal amplitude which exceeds the supply voltage without attenuation.

Manuscript received October 20, 2008.
Manuscript revised January 20, 2009.

[†]The authors are with the Graduate School of Advanced Sciences of Matter, Hiroshima University, Higashihiroshima-shi, 739-8530 Japan.
a) E-mail: masui@dsl.hiroshima-u.ac.jp

DOI: 10.1587/transele.E92.C.828

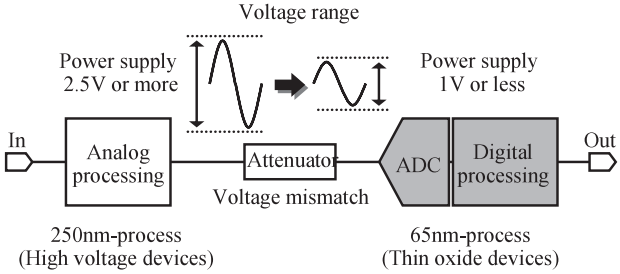


Fig. 1 Proposed beam former.

2. Delta Amplifier (DeltAMP)

2.1 DeltAMP Principle

The principle of DeltAMP is compared with a conventional AMP in Fig. 2. The DeltAMP consists of an AMP, a modulator placed in the virtual ground and capacitors for a feedback path. When the input signal amplitude exceeds analog range, a conventional AMP clips output wave forms. On the other hand, the DeltAMP folds the output wave forms by controlling the modulator according to a crossing timing of DeltAMP output (Aout+, Aout−) and the reference voltages (Vref_H, Vref_L). Since the input paths switch each phase, DeltAMP alternately puts out a reverse-polarity as shown in Fig. 2. As a result, the DeltAMP compresses the output voltage within Vref_H-Vref_L (Vref). The maximal signal compressibility, which is the ratio of input amplitude (Ain) to output amplitude (Vref), is limited by a unity frequency of AMP (funity) and a maximal modulator control frequency (fmod). The fmod is given by

$$f\mathrm{mod} = \pi \cdot fin \cdot Ain \cdot Gain/Vref(\leq funity) \quad (1)$$

where fin is input frequency and Gain is loop gain of DeltAMP. When fmod = funity, the maximal signal compressibility (Vref/Ain) is given by

$$Vref/Ain = \pi \cdot fin \cdot Ain \cdot Gain/funity \quad (2)$$

The DeltAMP can amplify larger signal amplitude than the supply voltage range and process the signal like a conventional amplifier by reconstructing output waves in extremely low voltage supply.

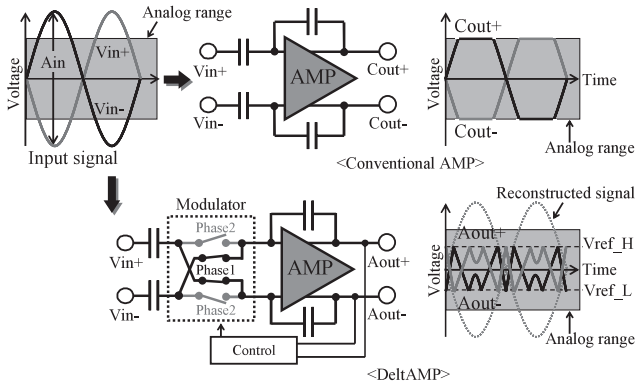


Fig. 2 Principle of DeltAMP.

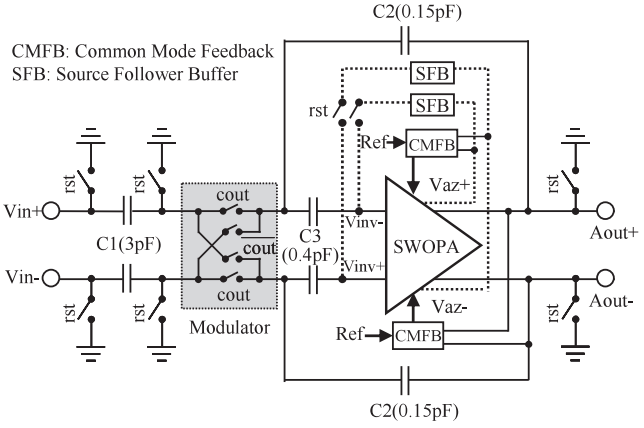


Fig. 3 Schematic of DeltAMP.

2.2 DeltAMP Architecture

Figure 3 shows a schematic of the DeltAMP which consists of a fully-differential switched op-amp (SWOPA), capacitors (C1, C2, C3) and a modulator. The signal amplitude of the modulator operated at the virtual ground is compressed into a 1/gain. In addition, the virtual ground voltage can be set to the proper level [6]. Therefore the modulator placed at the virtual ground is implemented by NMOS switches. The waveform of Aout is folded back within the range of Vref_H–Vref_L. In consequence, the reconstructed equivalent output amplitude (Ain × Gain) of DeltAMP can exceed the supply voltage.

In order to eliminate the dc offset voltage, the DeltAMP is equipped with an autozeroing scheme. During the autozeroing (rst) phase, the outputs of SWOPA are connected to its input using dotted lines as shown in Fig. 3. The paths are activated on the initial phase and the detected dc offset voltage is stored in the hold capacitor C3.

Since Vgs (gate-source voltage) has to be designed to be nearly as low as the Vth in a low supply voltage, the *gm* and an amplifier gain are reduced. Even though cascode amplifiers are widely used to improve a gain, it results in decreased voltage range. On the other hand, a cascade amplifier can improve the gain regardless of the supply voltage. However, multi-poles are generated in circuit nodes and it is difficult to ensure a sufficient phase-margin. Therefore the three stage cascade SWOPA, as shown in Fig. 4, with a special phase compensation technique is applied in this design. The stability of the SWOP is attained utilizing two phase-compensation techniques. To prevent deterioration of Mirror effect due to low gain of the second stage, a new phase-compensation implemented by a dummy AMP and C5 is applied, in addition to the conventional ones with C4 and R1. Thus the combined use of two phase-compensation techniques boosts the pole split effect.

The SWOPA has 4 outputs in order to configure the autozeroing operation. Although these outputs have offset voltages, these offset voltages can be disregarded. This is because the first stage offset voltage is predominant in the SWOPA.

Figure 5 shows the schematic of the Common-mode feedback circuit (CMFB). The output common-mode level of the SWOPA is detected using a resistive divider and compared with the reference voltage of 250 mV (= Vdd/2). It is returned to the feedback nodes COM of the SWOPA in Fig. 4.

Figure 6 shows the block diagram of DeltAMP with the folding control circuit, ATC. The ATC consists of two window comparators #1 and #2, each of which is two differential amplifiers with a switched capacitor auto-zeroing scheme, an OR logic and a Toggle-Flip-Flop (T-FF) as shown in Fig. 7. The window comparators #1 and #2 operate in an interleave scheme. While the window comparator #1 operates in comparison, the #2 samples the dc offset voltage of amplifiers. When the Aout crosses the reference voltage (Vref_H or Vref_L), the window comparator #1 outputs "high" and ATCout is toggled. Hence the operation of window comparator #1 and that of window comparator #2 are switched. A lowest input frequency is determined by a leak current and a capacitor value.

The ATC requires an asynchronous comparator. Therefore a dynamic comparator which operates by synchronizing with a clock can not be adapted. We adopted a cascode amplifier which operates continuously. A schematic of the differential cascade amplifier is shown in Fig. 8. If a conventional amplifier (Fig. 8(a)) is used as the comparator, the amplifier always consumes the current. To solve the problem, we use the amplifier without a tail current source as shown in Fig. 8(b). It does not have constant current flow and consumes short-circuit current only when the input signal and reference voltage are crossing. The amplifier is suitable for ATD architecture because of low power consumption.

2.3 Simulation Results

Figure 9 shows frequency characteristics of the SWOPA. When the conventional phase-compensation which is implemented by R1 = 18 kohm and C4 = 1 pF in Fig. 4 is used, the phase margin is 29 degrees as shown in Fig. 9(a). Even if the large capacitor was used in the SWOPA, a pole split was not

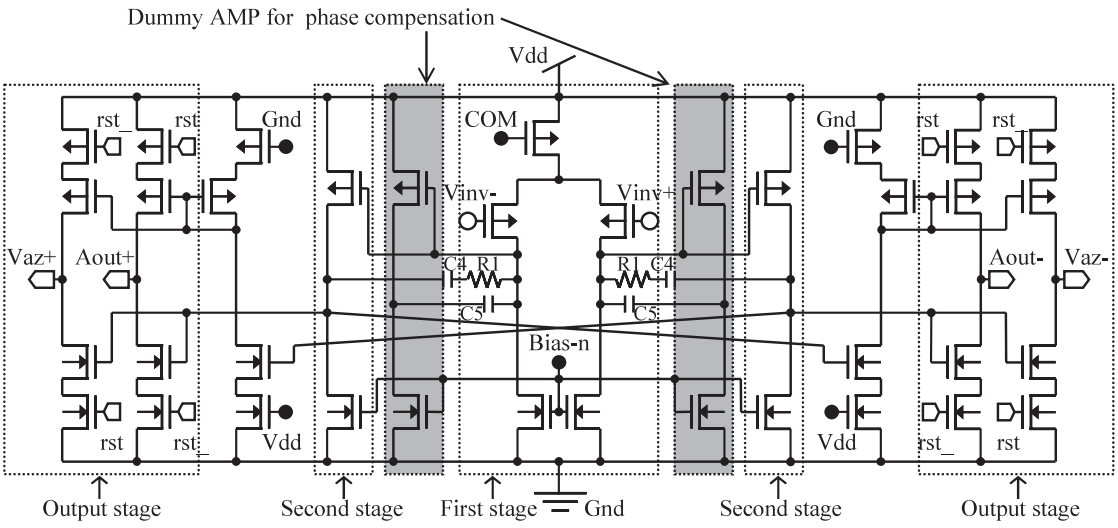


Fig. 4 Schematic of SWOPA.

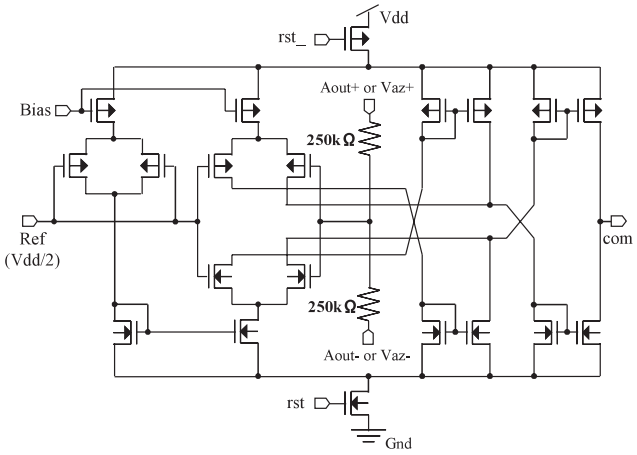


Fig. 5 Schematic of CMFB.

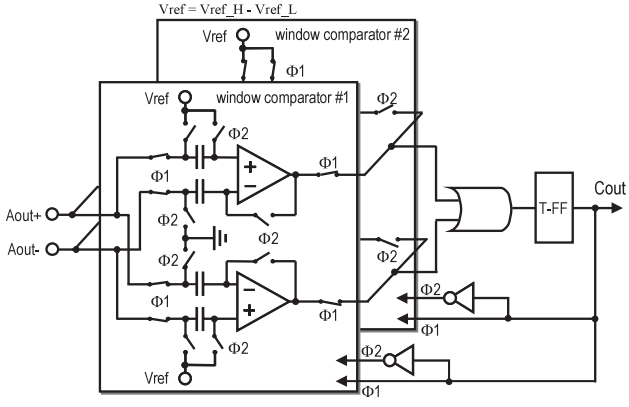


Fig. 7 Schematic of the A-to-T Converter with interleaving operation.

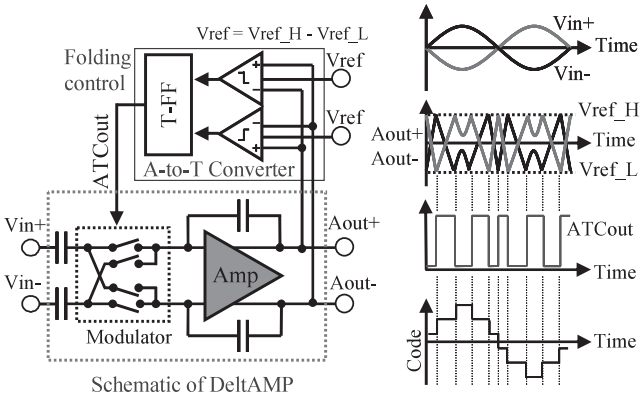


Fig. 6 Block diagram of DeltAMP with folding control circuit.

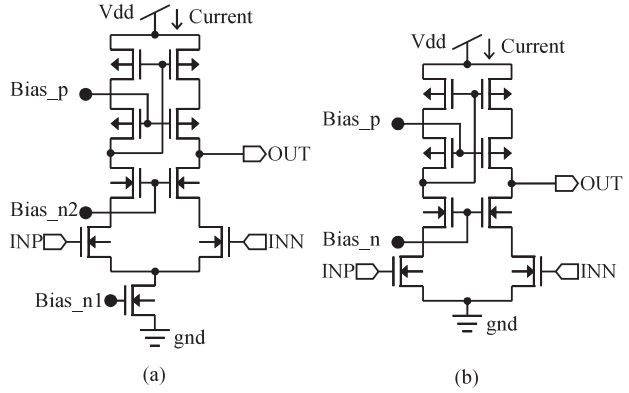


Fig. 8 (a) Conventional cascode amplifier, (b) Proposed cascode amplifier.

improved. On the other hand, when the combination of two techniques for compensation is used, the phase margin is 71 degrees as shown in Fig. 9(b). These results indicated the combination of two types of compensation boosts the pole split.

Figure 10 shows output waveforms of the comparator used in the ATC. The comparator works only when the difference of two inputs is small as shown in Fig. 10(a). In addition, Fig. 10(b) shows current consumption correspond-

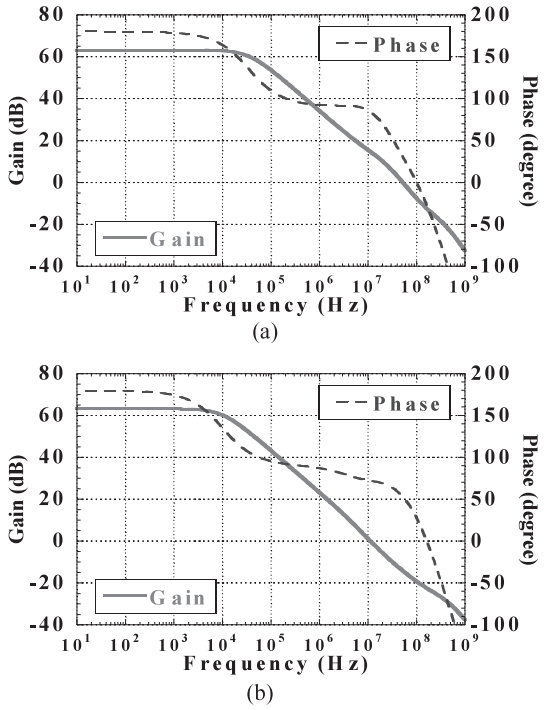


Fig. 9 Frequency response of SWOPA with traditional compensation, (b) Frequency response of SWOPA with a combination of two types of compensation.

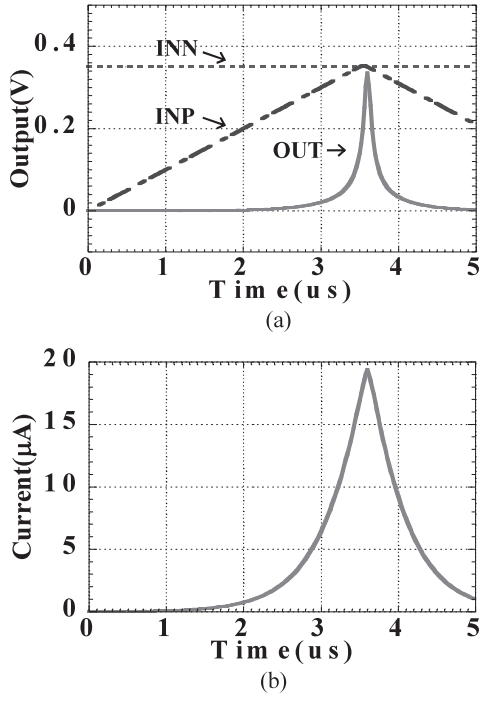


Fig. 10 (a) Output waves of amplifier that works as comparator, (b) Current consumption of amplifier.

ing to Fig. 10(a). The amplifier consumes the short-circuit current of 19.4 μA when the two inputs signals cross. If the conventional amplifier (Fig. 8(a)) is used as a comparator, the total current of 4 amplifiers in ATC is 77.6 μA (19.4 $\times$

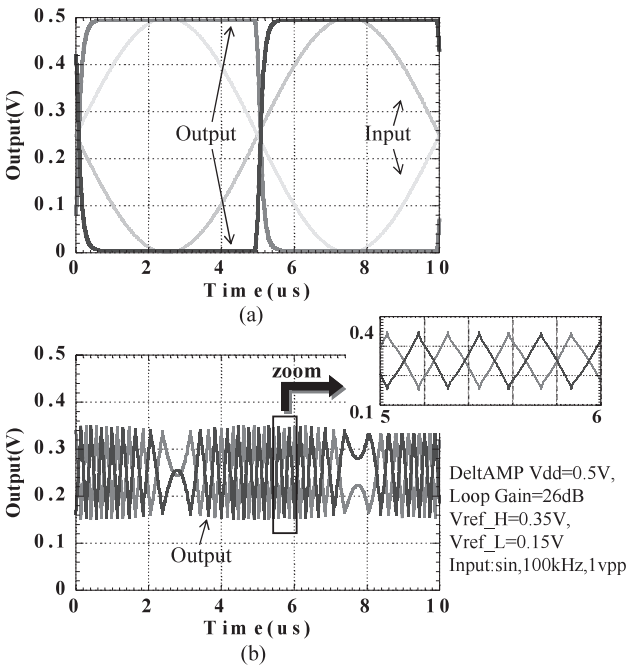


Fig. 11 (a) Output waves of conventional AMP (b) Output waves of DeltAMP with modulation.

4). On the other hand, the proposed amplifier does not have a short-circuit current in the compared operation. Thus the total current of 4 amplifiers in ATC is 46.6 μA. The consumption current was reduced by 42.5% with the proposed amplifier.

Figure 11 shows the simulation results of the DeltAMP. The DeltAMP was operated with a 26 dB loop gain and 1 Vpp input signal amplitude at a 0.5 V supply voltage. The output waves of the conventional AMP are shown in Fig. 11(a). The outputs of the AMP are clipped at the supply voltage. On the other hand, the DeltAMP folds the output waves between Ref_H and Ref_L as shown in Fig. 11(b). The simulation results indicated that the DeltAMP can process large signal amplitudes which the conventional AMP can not. Even a large input, greater than the supply voltage, is processed without an attenuator.

3. Deltamp with Reconstruction Circuit

The folded delta signal of the DelAMP output has to be reconstructed to the ordinal signal. This reconstruction should be processed in the digital domain. For this purpose, we propose a reconstruction circuit in an analog-digital merged technique. The circuit is called Analog-Time-Digital Converter (ATD) which is composed of ATC and Time-to-Digital Converter (TDC) [7], [8].

3.1 Circuit Configuration and Operation

In the case that amplified input swing (*Vin*) is larger than *Vref/Gain*, the ATC detects timings that Aout crosses with Vref (Vref_H and Vref_L) as shown in Fig. 12, and the

timings are converted to digital code by an asynchronous up/down counter. The output of the counter is synchronized by an external clock. The clock frequency determines the sampling rate.

In the case that input swing (*Vin*) is smaller than *Vref/Gain*, ATCout does not operate. In this case, DeltaAMP output (Aout) can be converted to digital code by adding intermediate comparator levels for ATD as shown in Fig. 13. The multi-bit ATD which has multiple intermediate comparator levels can respond to small input swings and improve the voltage resolution in the digital domain.

3.2 Signal to Noise Ratio (SNR)

In the ATD, SNDR can be decided by the equivalent voltage resolution and the over sampling ratio (OSR). The variation of input signal is amplified and reconstructs in the digital domain, and the equivalent voltage resolution in the digital domain is determined by the loop gain of DetlAMP (Gain) and Vref. In single-bit ATD, Vref is (Vref_H-Vref_L) as shown in Fig 12. In multi-bit ATD, Vref is (Vref_n+1-Vref_n) as shown in Fig 13. In addition, the ratio of fc (clock frequency of the counter) to 2 × fb (signal bandwidth) corresponds to the OSR in ATD. From the above, the SNR is given by

$$S/N(\mathrm{dB}) = 6.02\log_2(Ain \cdot Gain/Vref) + 1.76 + 10\log_{10} OSR \quad (3)$$

where Ain is input amplitude. The SNR of the ATD can be improved by increasing the Gain, number of intermediate comparators and OSR.

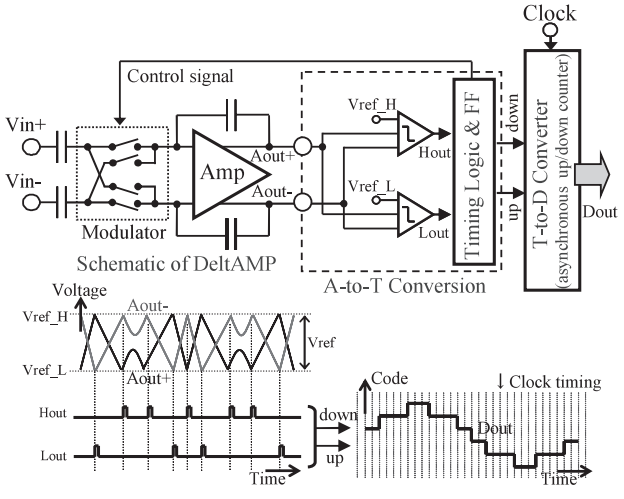


Fig. 12 Single-bit ATD.

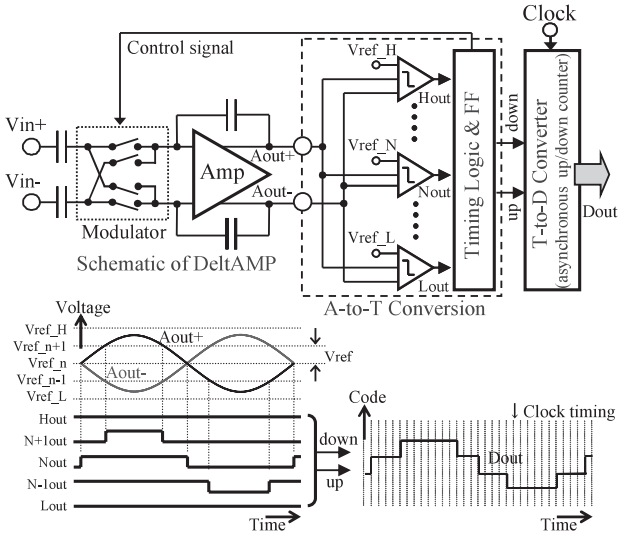


Fig. 13 Multi-bit ATD.

4. Measurement Results

The DeltAMP test chip was designed and fabricated with a 90 nm CMOS process. ATC was designed to have two comparator levels (VrefH and VrefL). The micrograph of the chip is shown in Fig. 14. The chip area is $500 \times 750\,\mu\mathrm{m}^2$. The TDC operation is implemented using a digital oscilloscope which detects transition of ATCout and counts the pulse width.

Figure 15 shows the measured output waveforms of DeltAMP with 26 dB gain and ATC when a 100 kHz, 1.0 Vpp differential sinusoidal input is applied at 0.5 V supply voltage. The reference voltages Vref_L and Vref_H are 0.15 V and 0.35 V, respectively. Even if the input signal exceeds the supply voltage, the output of DeltAMP is folded in between the reference voltages. The output bit stream obtained by using the TDC with 1ns time resolution, was demodulated into its original waveform by MATLAB. The output PSD of ATD is shown in Fig. 16. The noise floor increase of less than 20 kHz is caused by the number of FFT points, it is limited by the memory of the digital oscilloscope.

A delay of the window comparator and switches causes odd-order harmonic distortions in the signal which is reconstructed in the digital domain. The delay is proportional to the inclination of the input signal (= Δvoltage/Δtime). When the input frequency decreases, the distortion is improved as

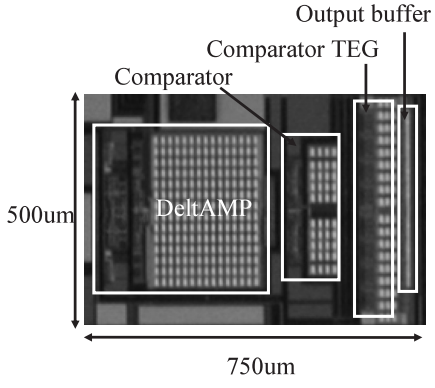


Fig. 14 Chip micrograph.

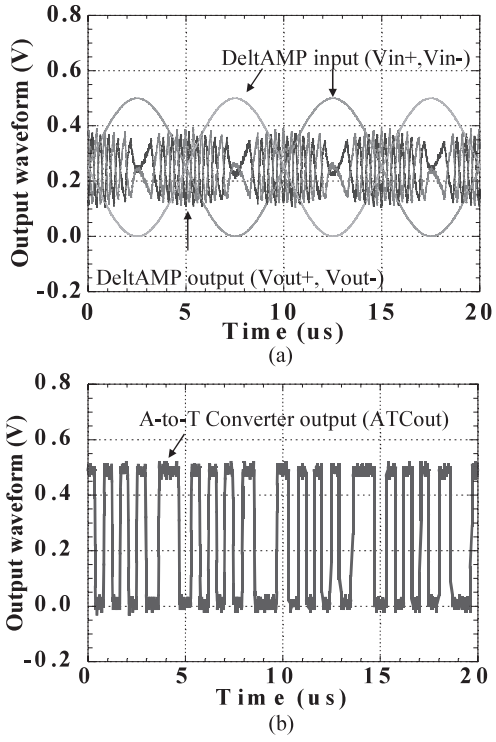


Fig. 15 (a) Input and output waveforms of DeltAMP, (b) Output waveforms ATC.

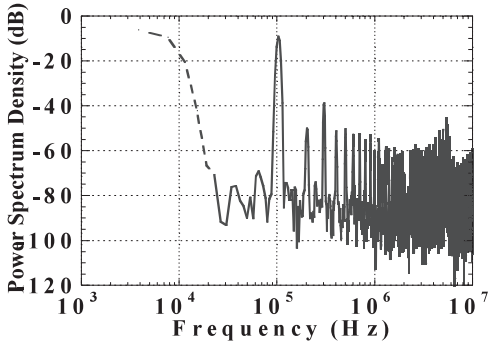


Fig. 16 Output spectrum of ATD with 100 kHz, 0.5 Vpp input.

shown in Fig. 17. In addition, to reduce the delay by using small MOS devices the distortion is improved. Measured SNR vs. clock frequency of TDC is shown in Fig. 18. The differential sinusoidal input voltage is 1 Vpp and the frequency is 100 kHz. The supply voltage is 0.5 V. The SNR is improved by up to 60 dB according to the increase of the clock frequency. The SNR versus input amplitude curve is illustrated in Fig. 19. The SNR data when the input swing level is smaller than (Vin/Gain) is not evaluated in the test chip. The differential signal amplitude four times the power-supply voltage can be processed due to the DeltAMP. The ADC achieved 62 dB SNR with 100 kHz signal, 2.0 Vpp input amplitude and 120 kHz bandwidth. The measured power consumption is as low as 150 μW (DeltaAMP: 120 μW and ATC: 30 μW) at a supply voltage of 0.5 V.

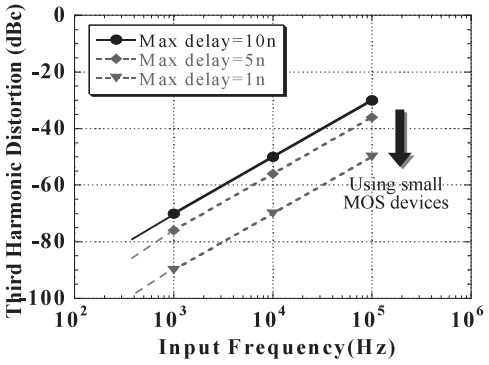


Fig. 17 Theory value of third harmonic distortion.

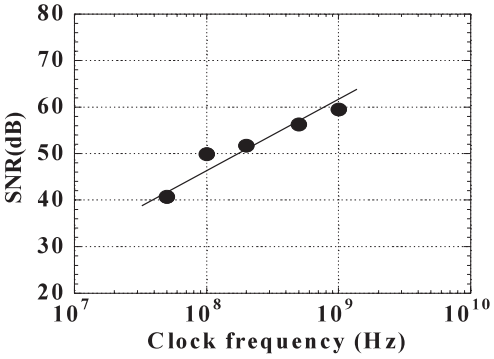


Fig. 18 SNR versus clock frequency of TDC.

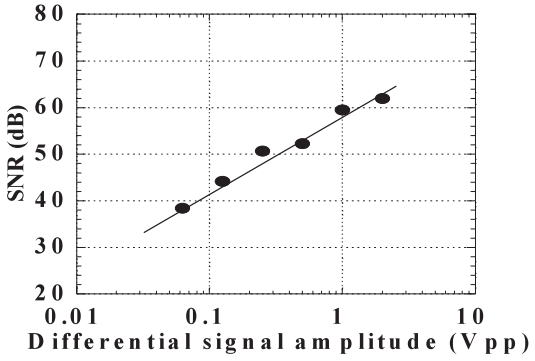


Fig. 19 SNR versus input amplitude.

5. Conclusion

To solve the voltage mismatch problem, DeltAMP is proposed. It can accept a large signal amplitude which exceeds the supply voltage by folding input signal without attenuation. For reconstruction of the folded DeltAMP output signal, we propose a reconstruction circuit ATD using time-to digital conversion techniques. A DeltAMP test chip with a 90 nm CMOS technology achieved an input voltage range of 2.0 Vpp, SNR of 62 dB at a signal bandwidth of 120 kHz, and power of 150 μW at a 0.5 V supply. This architecture will be advantageous to various applications which require a high-dynamic-range at low supply voltage and low power

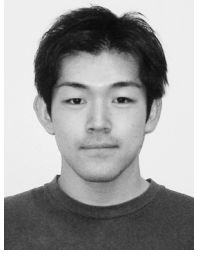
operation.

Acknowledgments

This research was supported by the Semiconductor Technology Academic Research Center (STARC). We would like to thank Drs. K. Mashiko, K. Gotoh, T. Taya, J. Nakatsuka, and M. Hamada for helpful discussions, and also to thank the VLSI Design and Education Center (VDEC), and the University of Tokyo for the offer of chip fabrication program.

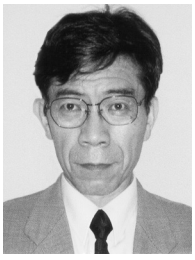
References

[1] H. Ballan, "Design and optimisation of high voltage analog and digital circuits built in a standard 5 V CMOS technology," Proc. Custom Integrated Circuits Conference, pp.574–577, San Diego, CA, USA, May 1994.
[2] M. Steyaert, et al., "Digital communication systems: the problem of analog interface circuits," Proc. Solid-State Circuits Conference, 2005. ESSCIRC 2005, pp.423–426, Grenoble, France, Sept. 2005.
[3] T. Cougar and V. Eaton, Design and implementation of High-Volatge CMOS Devices in a 0.8 μm 5 V CMOS Process, Thesis, Washionton State University, Aug. 1998.
[4] D. Pan, et al., "A low voltage to high voltagelevel shifter circuit for MEMS application," Proc. Biennial University-Government-Industry Microelectronics Symposium, pp.128–131, July 2003.
[5] D. Seo, et al., "High-voltage-tolerant analog circuits design in deep-submicronmeter CMOS technologies," IEEE Trans. Circuits Syst. I, vol.54, no.10, pp.2159–2166, Oct. 2007.
[6] T. Yoshida, et al., "A 1 V low-noise CMOS amplifier using autozeroing and chopper stabilization technique," IEICE Trans. Electron., vol.E89-C, no.6, pp.769–774, June 2006.
[7] M. Lee and A.A. Abidi, "A 9b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifiers a time residue," Proc. Symp. on VLSI Circuits, pp.168–169, June 2007.
[8] T. Komuro, J. Rivoir, K. Shimizu, M. Kono, and H. Kobayashi, "ADC architecture using time-to-digital converter," IEICE Trans. Electron. (Japanese Edition), vol.J90-C, no.2, pp.125–133, Feb. 2007.



Yoshihiro Masui received the B.E. and M.E. degrees in electronics engineering from Shibaura Institute of Technology and Hiroshima University, Japan, in 2003 and 2005, respectively. He is currently a doctoral candidate at the Graduate School of Advanced Sciences of Matter, Hiroshima University.

Takeshi Yoshida received the B.E., M.E. and D.E. degrees in electrical engineering, all from Hiroshima University, Japan, in 1994, 1996 and 2004, respectively. From 1996 to 2001, he was with the System Electronics Laboratories, Nippon Telegraph and Telephone Corporation. He is currently an assistant professor at the Graduate School of Advanced Sciences of Matter, Hiroshima University. His research focus is low-voltage analog circuit design for low-noise systems. Dr. Yoshida is a member of the Institute of Electrical and Electronics Engineers.



Atsushi Iwata received the B.E., M.S. and Ph.D. degrees in electronics engineering from Nagoya University, Nagoya, Japan, in 1968, 1970 and 1994 respectively. From 1970 to 1993, he was with the Electrical Communications Laboratories, Nippon Telegraph and Telephone Corporation. Since 1994, he has been a professor of Electrical Engineering at Hiroshima University. His research is in the field of integrated circuit design where his interests include, circuit architecture and design techniques for analog-to-digital and digital-to-analog converters, digital signal processors, ultra high-speed telecommunication IC's, and large-scale neural network implementations. He received an Outstanding Panelist Award at the 1990 International Solid-State Circuits Conference. Dr. Iwata is a member of the Institute of Electrical and Electronics Engineers.