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A Neural Recording Amplifier with Low-Frequency Noise Suppression

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SUMMARY To detect neural spike signals, low-power neural signal recording frontend circuits must amplify neural signals with below 100 μV amplitude and a few hundred Hz frequency while suppressing a large DC offset voltage, 1/f noise of MOSFETs, and induced noise of AC power supply. To overcome the problem of unwanted noise at such a low signal level, a low-noise neural signal detection amplifier with low-frequency noise suppression scheme was developed utilizing a new autozeroing technique. A test chip was designed and fabricated with a mixed signal 0.18-μm CMOS technology. The voltage gain of 39 dB at the bandwidth of the neural signal and the gain reduction of 20 dB at AC supply noise of 60 Hz were obtained. The input equivalent noise and power dissipation were 90 nV/root-Hz and 90 μW at a supply voltage of 1.5 V, respectively.

key words: *neural recording amplifier, neural signal sensing LSI, 1/f noise, autozero technology*

1. Introduction

Simultaneous neural signal sensing from many neurons in the brain has various applications ranging from the study of biological neural networks to the development of medical treatments such as a brain-machine interface and/or a biopotential monitoring [1]–[4]. Figure 1 shows the connection diagram of neurons and probes. Due to electrochemical effects at the neuron-probe interface, DC offsets of about 1 V are measured across differential probes. Typical neural spike signals have an amplitude of around 100 μV, a low frequency (~5 kHz) and a firing rate of a few times per second when using extracellular probes as shown in Fig. 1. The neural signal that a neural recording system detects is attenuated by the extracellular fluid and polarization.

In order to better detect weak neural signals, neural recording systems which included a low-noise amplifier with high input impedance have been developed [5], [6]. Generally, the neural signals have been observed in vitro and in a noiseless measurement environment when it is not possible to use a high-density assembly like a Utah Microelectrode Array (UMA) [6] and a Michigan Microelectrode Array [7]. However, the neural recording system, which has cables about 15-cm long connecting the electrodes and the circuit, must detect neural signals buried in an induced AC supply noise (hum noise), in order to observe neural signals of the measured objects under real activity [8]. This paper reports on a new neural recording amplifier which suppresses the unwanted environmental noise.

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2. Amplifier Design

Figure 2 shows the system architecture of the neural recording system. The system consists of the proposed low-noise neural recording amplifier and a wireless neural recording system-on-a-chip (SoC). The SoC reported in [9] includes low-noise amplifiers, 10-bit ADCs, a control unit and an RF transmitter. The proposed amplifier amplifies the neural spike signal in the cerebellum of a goldfish and sends the amplified signal to the SoC. Thus a low-noise performance and a suppression of induced AC supply noise on the con-

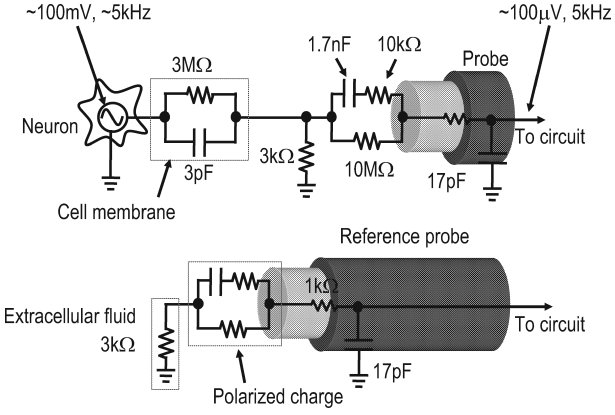

Fig. 1 Connection diagram of neuron and probes.

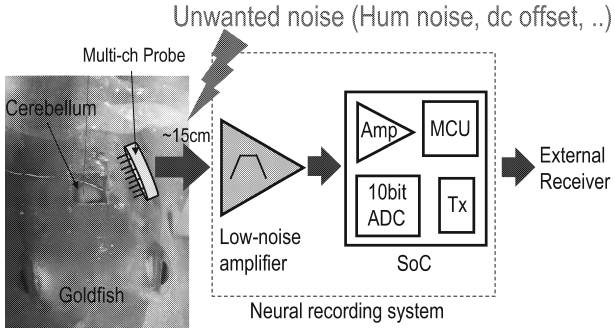

Fig. 2 System architecture of the neural recording system.

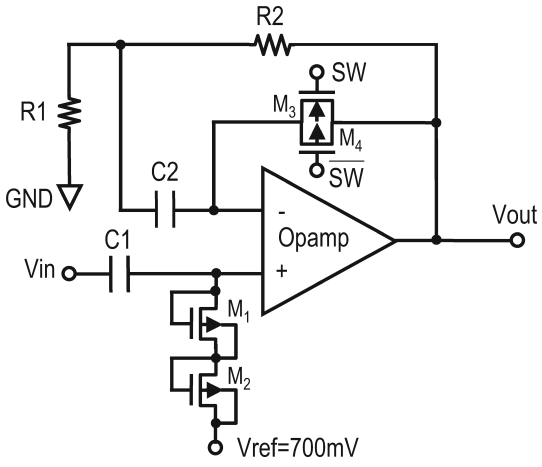

Fig. 3 Schematic of the proposed amplifier.

necting cable are required for the proposed amplifier.

The schematic of the proposed amplifier is illustrated in Fig. 3, which consists of an opamp and feedback circuit. The amplifier equips an AC coupled capacitor C1 and resistors implemented by MOSFETs operated in subthreshold at the input nodes [10], thus the amplifier realized high input impedance and fixed the input DC level of the amplifier to the reference voltage. Designed parameters are as follows: C1 = 1.2 pF, C2 = 5.2 pF, R1 = 1 kΩ and R2 = 80 kΩ. Figure 4 shows a schematic of the opamp used in the proposed amplifier. The input pair of the opamp is chosen to be a p-channel MOSFET with a large gate area to minimize the 1/f noise contribution.

The operation of the proposed amplifier is described as follows. Figure 5(a) shows the waveform of input signal Vin. Firstly, the CMOS switch (SW) shown in Fig. 3 is turned on, and the capacitor C2 is charged to a voltage of Vin+Voff+Vfn by a voltage follower configured by the opamp, where Voff is an offset voltage of opamp and Vfn is a 1/f noise of the opamp. While the SW is 'ON' the sampling period and the output of the amplifier is set to around the reference voltage Vref as shown in Fig. 5(b). Secondly, the SW is turned off, the voltage of Vin+Voff+Vfn is sampled and held with the C2, and the difference between the sampled voltage and the input signal voltage is amplified (Fig. 5(b)). Finally, the output voltage (Vout) which modulated with the modulation period as shown in Fig. 5(b), is reconstructed in digital domain by accumulating Vout at each sampling timing (Fig. 5(c)).

The proposed amplifier, which behaves as a differentiation circuit, can amplify only the variation of the input signal by utilizing the autozero technology as shown in Fig. 5(b), thus it suppresses not only the low frequency noise such as 1/f noise but also the AC supply noise and the electrochemical effects by using the differential operation. A suppression ratio K of input signal amplitude in the proposed amplifier is given by

$$K = fm/fin \times \pi \quad (1)$$

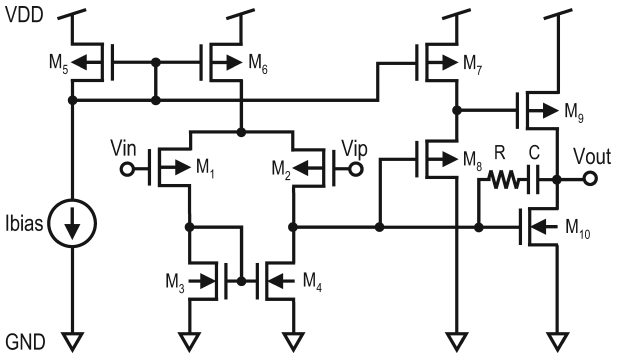

Fig. 4 Schematic of opamp used in proposed amplifier.

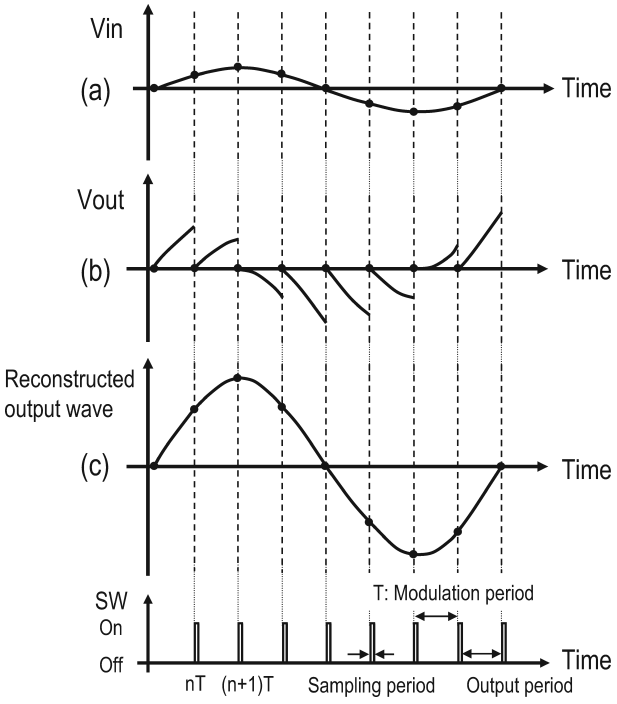

Fig. 5 Operating principle of the proposed amplifier and a timing chart.

where the fin is an input signal frequency and the fm is a modulation frequency. The fm is defined as 1/ (modulation period). In order to realize a 20 dB suppression of the AC supply noise at 60 Hz, the fm needs 32 times higher frequency than the AC supply noise. Therefore, the required modulation frequency is higher than 2 kHz.

3. Simulation Results

The proposed amplifier was designed with a 0.18-μm mixed-signal CMOS process with a metal-insulator-metal (MIM) capacitor. The circuit performances were evaluated by SPICE simulation. The opamp used in the proposed amplifier is designed to have a 72 dB open-loop gain, −3 dB bandwidth of 2 kHz and 6 MHz unity-gain frequency with a capacitor load of 10 pF.

The simulated waveforms of a conventional opamp and the proposed amplifier with input signal, which mixed the

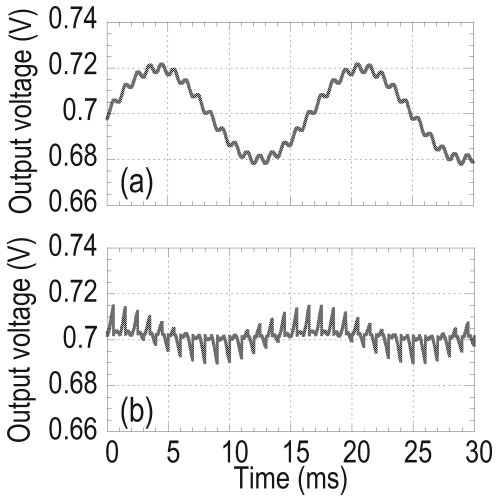

Fig. 6 Simulated output waveforms of (a) the opamp and (b) the proposed amplifier.

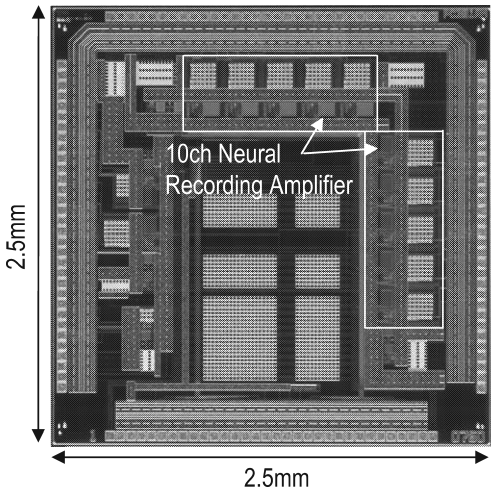

Fig. 7 Micrograph of 2.5 x 2.5 mm chip containing 10ch neural recording amplifier.

AC supply noise (1 mV, 60 Hz) and a pseudo neural signal (100 μV, 1 kHz), is shown in Fig. 6. The proposed amplifier is operated with the modulation frequency of 2 kHz (with a sampling period of 2 μs and an output period of 498 μs). The proposed amplifier suppresses the AC supply noise and amplifies the neural signal as shown in Fig. 4(b). Moreover, the input impedance of the proposed amplifier obtained larger than 1 GΩ.

4. Experimental Results

The chip micrograph of the proposed 10ch low-noise neural recording amplifier chip fabricated in a 0.18-μm CMOS technology is shown in Fig. 7. The amplifier layout area of 1ch is 250 $\times$ 450 μm.

The simulated and measured frequency response of the proposed amplifier is shown in Fig. 8. The proposed amplifier was operated with the modulation frequency of 2 kHz (with a sampling period of 2 μs and an output period of 498 μs) at a supply voltage of 1.5 V. The proposed amplifier has a band-pass-filter characteristic; it has a high-pass pole of 600 Hz and a voltage gain of 36 dB from 1 kHz to 100 kHz. Consequently, the proposed amplifier suppressed the AC supply noise at 60 Hz to the neural signal by about 20 dB. The overshoot of the voltage gain at around 1 kHz appeared in the simulation and measurement results because of a resetting operation of the output waveforms shown in Fig. 5(b). However the overshoot is removed since the output waveforms are reconstructed as shown in Fig. 5(c). The other high-pass pole of around 10 Hz, given by a high-pass-filter, consists of C1 and MOS resistors shown in Fig. 3.

The measured input noise PSD of opamp used in the proposed amplifier and the proposed amplifier is shown in Fig. 9. The input noise PSD of opamp shows a typical 1/f noise spectrum, and the input noise PSD is 1.2 μV/root-Hz at 1 Hz. The proposed amplifier suppressed the input noise PSD at 1 Hz to less than 90 nV/root-Hz utilizing the

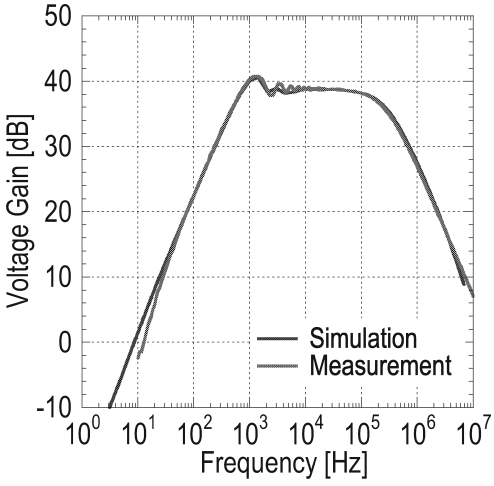

Fig. 8 Simulated and measured frequency response of the proposed amplifier.

autozeroing technique. The input noise PSD around 1 kHz of the proposed amplifier is larger than that of opamp; because the autozeroing increases the baseband noise floor, which is caused by the aliasing of the wideband noise that is inherent to the sampling process. However, it has an insignificant effect on a measurement of a neural spike signal (~10 kHz). The proposed amplifier has an equivalent input noise of 2.7 μV (~1 kHz), and 90 μW power consumption at a supply voltage of 1.5 V.

The measured output waveform of the opamp and the proposed amplifier with an input of a pseudo neural signal (amplitude of 5 mVpp and frequency of 500 Hz) is shown in Fig. 10(a). The output waveform was reset to around the reference voltage Vref of 0.7 V during every sampling period of 2 μs, thus the proposed amplifier only amplifies and outputs a variation of input signal during the output period. Figure 10(b) shows a waveform in a digital domain which reconstructed the output waveform of proposed amplifier

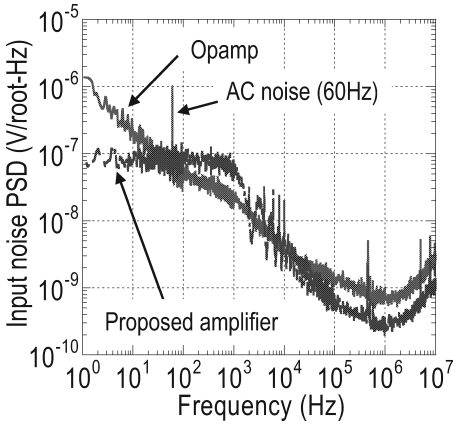

Fig. 9 Measured input noise PSD versus frequency of the opamp and the proposed amplifier with the modulation frequency of 2 kHz.

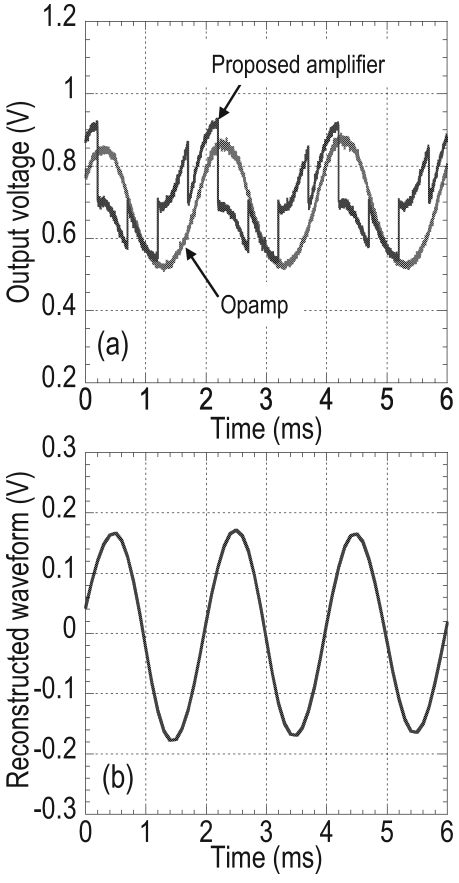

Fig. 10 (a) Measured output waveform of the opamp and the proposed amplifier with the input sine signal (amplitude of 5 mVpp and frequency of 500 Hz) and (b) reconstructed output waveform of the proposed amplifier.

shown in Fig. 10(a). The proposed amplifier can output the neural signal at 500 Hz without attenuation.

The measured output waveforms of the opamp and the proposed amplifier with a pseudo AC supply noise (amplitude of 50 mVpp and frequency of 60 Hz) are shown in Fig. 11. The proposed amplifier suppresses the AC supply noise of 60 Hz about 20 dB.

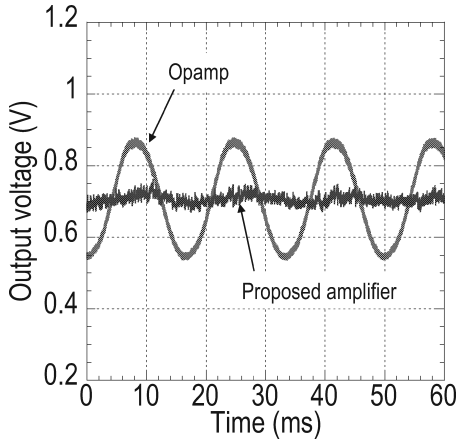

Fig. 11 Measured output waveforms of the opamp and the proposed amplifier with a pseudo AC supply noise (amplitude of 50 mVpp and frequency of 60 Hz).

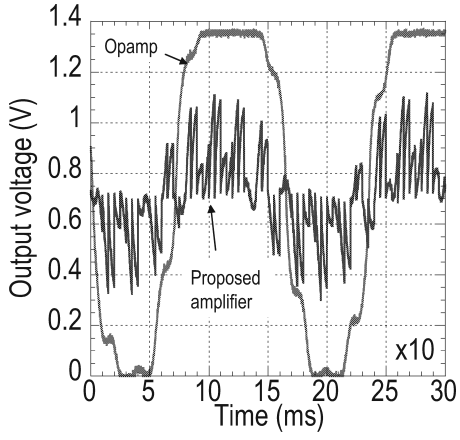

Fig. 12 Measured output waveforms of the opamp and the proposed amplifier with input signal, which mixed the AC supply noise (5 mV, 60 Hz) and pseudo neural signal (0.5 mV, 500 Hz).

The measured waveforms of the opamp and the proposed amplifier with input signal, which mixed the AC supply noise (5 mV, 60 Hz) and pseudo neural signal (0.5 mV, 500 Hz), is shown in Fig. 12. The output waveform of the opamp is clipped at the power supply; however the proposed amplifier suppresses the AC noise and folds the output signal between the supply rails.

To compare the performance of the proposed amplifier with that of the other ones reported in recent papers, we introduce the concept of noise efficiency factor (NEF). According to [11],

$$NEF = V_{ni,rms} \times (2I_{tot}/(\pi \times V_T \times 4kT \times BW)^{1/2} \qquad (2)$$

where $V_{ni,rms}$ is the equivalent input rms noise voltage, I_{tot} is the total amplifier supply current, V_T is the thermal voltage, and BW is the amplifier bandwidth in hertz. An amplifier using a single bipolar transistor (with no 1/f noise) has an NEF of one; all practical circuits have higher values. Fig. 13 shows a plot of the amplifier current versus the total equivalent input noise voltage per root bandwidth for published

Table 1 Measured performance characteristics of neural recording amplifier.

Parameter	Ref. [10](Neural)	Ref. [10](EEG)	This work
Process [μm]	1.5	1.5	0.18
Supply voltage [V]	±2.5	±2.5	1.5
Supply current [μA]	16	0.18	60
Voltage gain [dB]	40	40	39
Bandwidth [kHz]	7.2	0.03	100
Equivalent Input noise (μVrms)	2.2	1.6	2.7
Noise efficiency factor (NEF)	4	4.8	3.7

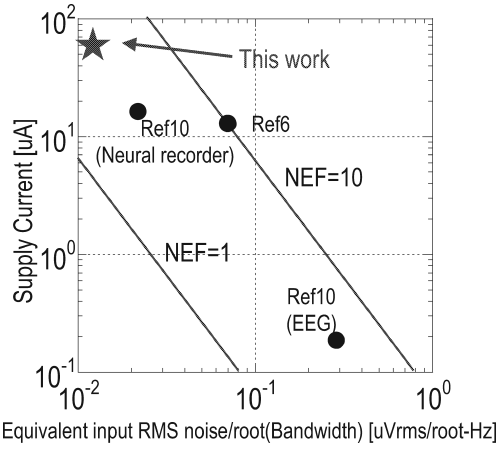

Fig. 13 Total current versus normalized equivalent input noise voltage for reported amplifiers (circle) and for this paper (star). Lines are contours of constant NEF.

neural recording amplifiers. Lines are contours of constant NEF. The proposed amplifier achieves comparable with the best of low NEF, which is reported neural recording amplifier [6], [10]. Table 1 summarizes the performance characteristics of the neural recording amplifier with other reported neural recording amplifier [10].

5. Conclusion

To suppress the AC supply noise and the low-frequency potential fluctuation of the polarized charge, the low-noise neural recording amplifier utilizing the autozero technique is proposed. The neural recording system based on the proposed technique suppresses the unwanted noises and it enables observation of the neural signals of measured objects during real activities in real environments. This technique has possibilities in practical application to state of the art health care as well as clarification of the relationship between the brain and real activities. The proposed amplifier fabricated with 0.18-μm CMOS technology achieved 20 dB reduction of the AC supply noise, equivalent input noise of 2.7 μV and 90 μW power consumption at a supply voltage of 1.5 V.

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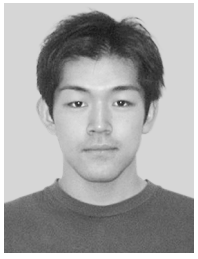

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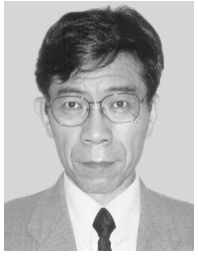

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