CMOS Gaussian Monocycle Pulse Transceiver for Radar-Based Microwave Imaging

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***Abstract*—A single-chip Gaussian monocycle pulse (GMP) transceiver was developed for radar-based microwave imaging by the use of 65-nm complementary metal oxide semiconductor (CMOS) technology. A transmitter (TX) generates GMP signals, whose pulse widths and −3 dB bandwidths are 192 ps and 5.9 GHz, respectively. A 102.4 GS/s equivalent time sampling receiver (RX) performs the minimum jitter, input referred noise, signal-to-nose-ratio (SNR), signal-to-noise and distortion ratio (SNDR) effective number of bits (ENOB) of 0.58 ps, 0.24 mVrms, 28.4 dB, 26.6 dB and 4.1 bits, respectively. The SNR for the bandwidth of 3.6 GHz is 36.3 dB. The power dissipations of transmitter and receiver circuits are 19.79 mW and 48.87 mW, respectively. The GMP transceiver module can differentiate two phantom targets with the size of 1 cm and the spacing of 1 cm by confocal imaging.**

***Index Terms*—CMOS, confocal imaging, equivalent time sampling, Gaussian monocycle pulse, microwave imaging, radar, transceiver, ultra-wide-band.**

Manuscript received August 12, 2020; revised September 29, 2020; accepted October 1, 2020. Date of publication October 7, 2020; date of current version December 30, 2020. This work was supported in part by the Research Center for Biomedical Engineering, Japan, Ministry of Internal Affairs and Communications (SCOPE#185008001), Japan, Support Center for Advanced Telecommunications Technology Research (SCAT), Japan, Nozomi-H Foundation, Japan, VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration with Cadence Corporation and Mentor Graphics Corporation. This paper was recommended by Associate Editor Prof. Shuenn-Yuh Lee. *(Corresponding author: Takamaro Kikkawa.)*

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Digital Object Identifier 10.1109/TBCAS.2020.3029282

I. Introduction

THE most commonly used modality for breast cancer screening is X-ray mammography. However, it causes ionizing radiation, resulting in the contraindications due to frequent examinations for young women. On the other hand, microwave imaging is a non-invasive technique to detect breast cancers because the microwave signal scatters at the interface between breast cancer and normal tissues without radiation exposure. It is attributed to the fact that the complex permittivity of breast cancer tissue is higher than those of normal breast tissues [1]–[3].

Many research groups have been devoted to develop microwave imaging systems [4]–[13]. Generally, there are two microwave imaging methods with respect to waveforms and algorithms. One is radar-based approach and the other is tomography. Klemm and Craddock *et al.* proposed a multi-static radar-based detection system. The impulse-radio-ultra-wide-band (IR-UWB) is used with the antenna array and a hemispherical dome in the range of 3.1 GHz–10.6 GHz [8], [9]. The system requires women to lie in prone position and set their breast pendants into the dome. The experiment was conducted using a vector network analyzer (VNA) and bank switches. The system used the delay and sum approach in the imaging process. On the other hand, the microwave tomography uses multi-frequencies to reconstruct the distribution of the breast dielectric properties [12]–[14]. Meaney *et al.* developed a 3D parallel-detection system with 16 vertically-oriented monopole array antennas [12]. The system used signal generator to transmit a continuous single frequency signal. A 3D iterative Gauss-Newton algorithm was utilized to reconstruct the dielectric distribution in the breast. However, the system required significant amount of time for computing. The systems above used off-the-shelf commercial equipment, resulting in large foot prints and heavy housing only acceptable for large hospitals. Portability with low power consumption is highly desired for frequent examination of breast cancer screening in any place.

In the prior works, a single-ended UWB radar system for Gaussian monocycle pulse (GMP) was developed using complementary metal oxide semiconductor (CMOS) integrated circuits (IC) and monopole antennas [15], [18], [20]. A CMOS GMP transmitter IC [15], [19] and a receiver IC with 4-bit flash analog-to-digital converter (ADC) plus track and hold (T/H) circuit [15], [21] were developed. Since the resolution of 4-bit ADC (1

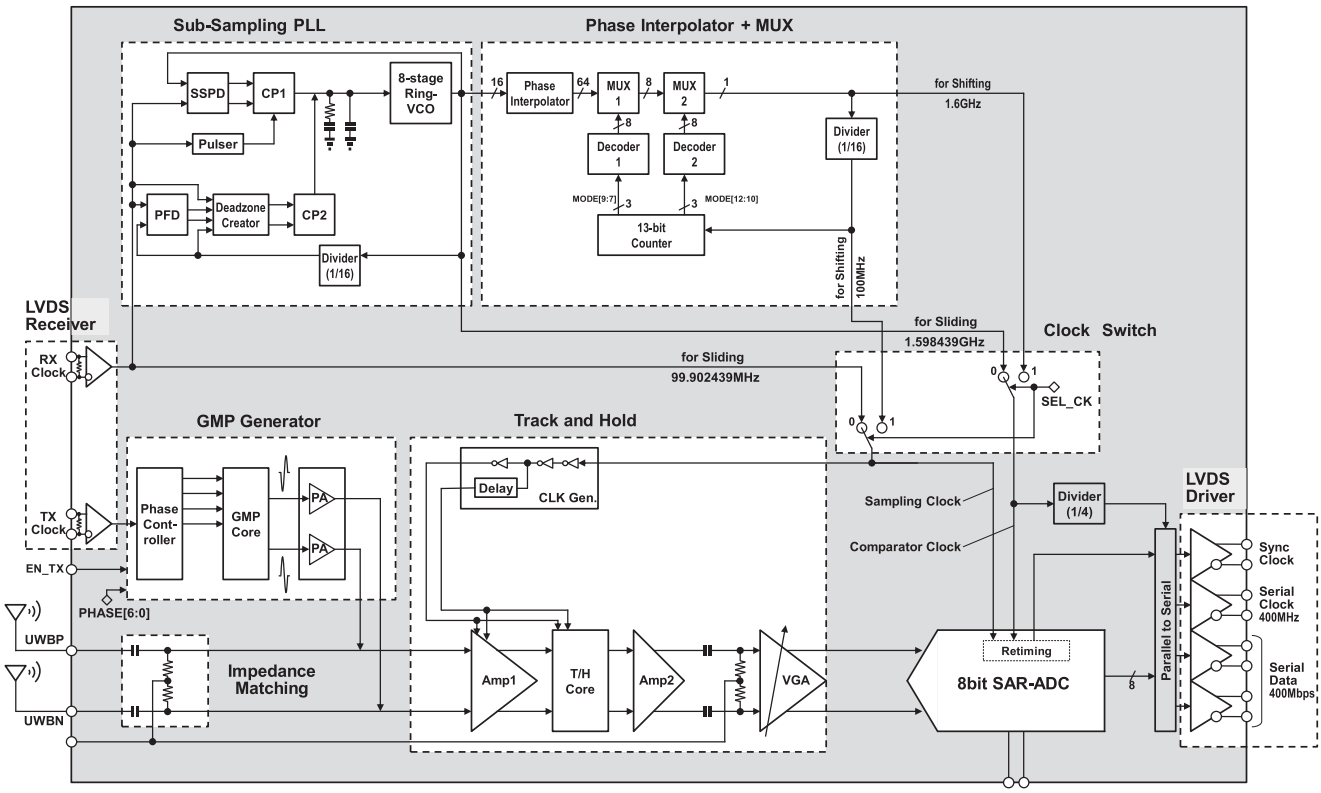


Fig. 1. Block diagram of a single-chip fully differential CMOS transciever for IR-UWB radar-based microwave imaging.

LSB = 62.5 mV @ 1V) was not sufficient for weak received signals, it failed to differentiate the peak of GMP. To solve the resolution issue, a 12-bit ADC IC (AD9233), a track and hold IC (HMC760LC4B) and an amplifier (AMP) IC (AD8352) were implemented in the previous prototypes [16]. We have succeeded the clinical trial for breast cancer detection using the prototype at the hospital [16], [17]. However, the drawback of the general-purpose IC was large power consumption, that is, 1.42 W for track and hold IC, 0.145 W for 12-bit-ADC IC and 0.21 W for AMP IC.

The goal of this work is to reduce the power consumption for a portable microwave imaging system. In this paper, a CMOS transceiver is described, which has a GMP transmitter and an 8-bit SAR-ADC with equivalent time sampling.

II. GMP Transceiver

In order to develop radar-based microwave imaging for breast cancer detection, the spatial resolution is set at 5 mm so that the pulse width of a transmitting GMP is designed at 200 ps with 10 ps time resolution (3 mm spatial resolution in the air). The GMP is generated by the combination of rising and falling edges of rectangular pulses using a logic circuit so that a 65 nm CMOS technology at $V_{DD} = 1.2$ V is used. The corresponding center frequency and the bandwidth are 5 GHz and 6 GHz, respectively. The amplitude of a transmitting GMP is set at 320 mVpp (−6 dBm). The attenuation of GMP in both antennas and the breast tissue is estimated approximately at −40 dB, so that the amplitude of the received GMP signal decreases to approximately −46 dBm. Since the thermal noise for the signal bandwidth of 6 GHz at 300°K is −76 dBm, the signal-to-noise ratio (SNR) is estimated at approximately 30 dB. To improve the SNR, an averaging technique with repeated measurement is necessary.

Fig. 1 shows a block diagram of a single-chip CMOS transceiver for IR-UWB radar. It is composed of a GMP generator, sampling clock generators, an impedance matching, a track and hold (T/H) and an 8-bit-successive-approximation-register analog-to-digital-converter (SAR-ADC). To keep the integrity of the GMP waveforms with high frequency clocks at input/output (I/O) interfaces, low voltage differential signaling (LVDS) is adopted.

The equivalent time sampling is developed by the use of either the sliding clock in the frequency domain or the shifting clock in the time domain. The sampling rate of 102.4 GS/s with 9.77 ps sampling period is developed. The shifting clock is generated by a sub-sampling phase locked loop (SS-PLL), an 8-stage ring voltage-controlled oscillator (VCO), phase interpolators (PI), multiplexers (MUX) and a divider (DIV). The sliding clock is generated by two crystal clocks with different frequencies.

A. GMP Generator

Figs. 2(a) and (b) show block diagrams of GMP core and a phase delay controller, respectively. GMP signals are generated based on the external 100 MHz crystal oscillator (KLO-628MA).

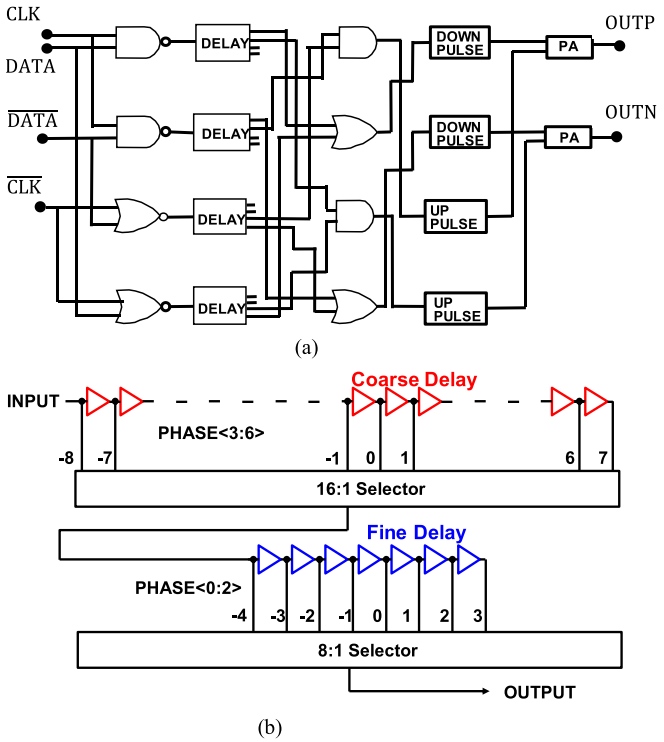


Fig. 2. Block diagrams of GMP generator. (a) GMP core. (b) Phase delay controller.

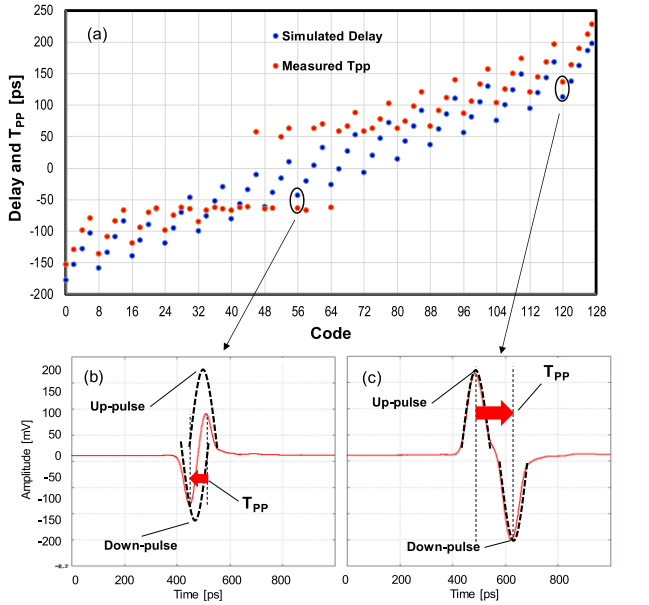


Fig. 3. (a) Simulated delay of phase controller and measured peak-to-peak time of GMP versus phase control code. (b) Waveforms of GMP with down-pulse-first (code_056). (c) Waveforms of GMP with up-pulse-first (code_120).

To form the GMP, the up-pulse and down-pulse are generated separately. The relevant schematic diagrams are detailed in Reference [19]. The GMP pulse width is controlled by the rise time and the fall time of the rectangular pulses, which depends on the gate length of the CMOS transistor in the GMP core. The gate length of 150 nm is designed for the target GMP pulse width of 200 ps. The phase delay of the input rectangular pulses is controlled by the phase controller, in which the combination of 4-bit coarse and 3-bit fine delays is controlled by $2^7 = 128$ codes.

Fig. 3 (a) shows the simulated delay between up- and down-pulses of the phase controller and the measured peak-to-peak time (T_{PP}) of GMP versus phase control code. The T_{PP} is controlled by 128 phase codes of the phase controller in the range from -200 to $+250$ ps. The measured T_{PP} is different from the simulated delay of the phase controller within $\pm$ 50 ps due to overlapping the delay with the peak-to-peak time as shown in Fig. 3(b), which is the waveforms of GMP with down-pulse-first for the code_056 of the phase controller. Fig. 3(c) shows the waveforms of GMP with up-pulse-first for the code_120, in which a hump of GMP is observed due to the longer T_{pp}.

The generated GMP waveform can be measured by using a wide-bandwidth oscilloscope at the UWBP and UWBN ports. A reference clock of 100 MHz and 1.2 Vpp is supplied to GMP generator circuit in the CMOS-LSI by a pulse generator (Agilent 81134A) and a generated GMP waveform is observed by a wide-bandwidth oscilloscope (Agilent 86100C and 86112A). The phase delay of the rectangular pulses of the phase controller was controlled by the register code to improve the distortion and amplitude of the GMP waveform. Measured GMP waveforms and fast Fourier transform (FFT) spectra are shown in Figs. 4(a) and (b), respectively.

The pulse widths, center frequency and amplitudes for the code_068 of the phase controller are 192 ps, 5.2 GHz and 280 mV pp (diff), respectively. The highest center frequency is obtained at the code_068. The effective amplitudes of the differential GMP signal is 396 mVpp (diff) after correcting the loss of a hybrid coupler for the measurement. The -3dB and -10dB bandwidths of GMP for the code_068 of the phase controller are 5.9 GHz (2.3–8.2 GHz) and 10.2 GHz (0.9–11.1 GHz), respectively.

On the other hand, the GMP of the code_098 has the pulse widths of 286 ps, the center frequency of 3.5 GHz, amplitude of 325 mV pp (diff), effective amplitudes of 460 mVpp (diff), -3dB bandwidth of 4.2 GHz (1.7–5.9 GHz) and -10 dB bandwidth of 6.8 GHz (0.7–7.5 GHz). The largest amplitude is obtained at the code_098.

B. Equivalent Time Sampling

The -3 dB bandwidth of the GMP with the pulse width of 192 ps is 5.9 GHz as shown in Fig. 4(b). However, the FFT spectrum is not the normal distribution but has the extended tail up to the necessary bandwidth of 20 GHz. To recover the GMP waveform after the ADC, the sampling frequency of twice as high as signal bandwidth is necessary. For the assumed minimum GMP pulse width of 100 ps, the sampling period of about 10 ps is selected by using equivalent time sampling (ETS) [21].

Fig. 5(a) shows a principle of the ETS by using shifting clocks in the time domain. Fig. 5(b) shows a principle of the ETS using the sliding clocks in the frequency domain. Figs. 6(a) and (b) are sampling clock generation block diagrams for shifting and sliding clocks, respectively. Table I shows the clock generation

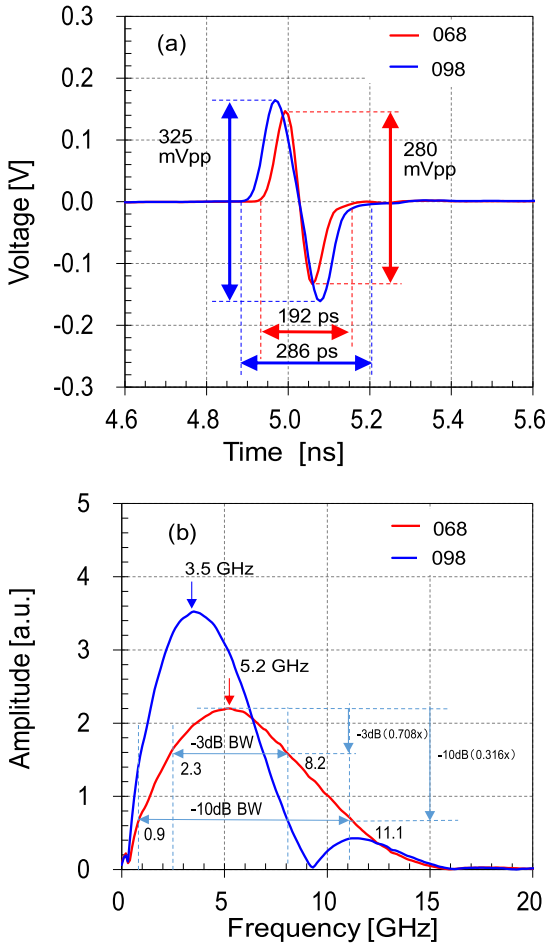


Fig. 4. Measured GMP waveform and FFT spectrum. (a) GMP waveforms for code_068 / 098. (b) FFT spectra for code_068 / 098.

TABLE I
CLOCK GENERATION SCHEMES

	Shifting Mode	Sliding Mode
Clock Generator	1.6 GHz	0
TX Crystal Clock Input	100 MHz Common	100 MHz
RX Crystal Clock Input		99.902439 MHz
ADC Sampling Clock	100 MHz Shifting	99.902439 MHz
ADC Comparator Clock	1.6 GHz Shifting	1.598439 GHz

scheme. The relative advantages of the shifting and sliding clocks are the reduced cost due to single crystal oscillator and the less deterministic jitter due to high precision crystal oscillators, respectively.

A 1.6 GHz 8-stage differential VCO generates 16 phases of 1.6 GHz clock for the shifting clock generator. A PI generates 64 phases of 1.6 GHz clock, a MUX selects 1 phase of 1.6 GHz clock, and a DIV (1/16) generates 1 phase of 100 MHz shifting clock. The received signal is sampled and digitized by T/H and 8-bit SAR-ADC with 100 MHz shifting clock and 1.6 GHz comparator clock as shown in Fig. 6(a). The phase and frequency are controlled by the sub-sampling PLL. The received GMP signal is down-converted to 1/1024 in the time domain.

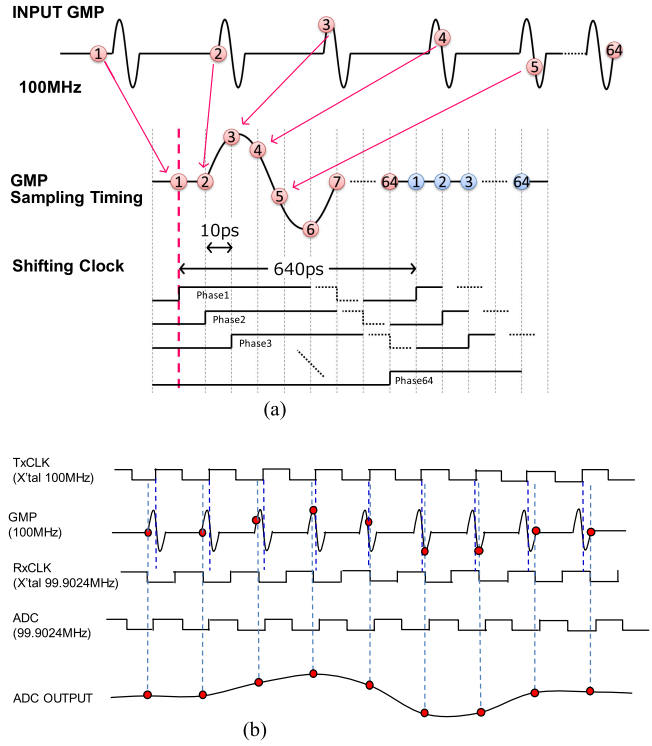


Fig. 5. Principle of equivalent time sampling. (a) Shifting clock. (b) Sliding clock.

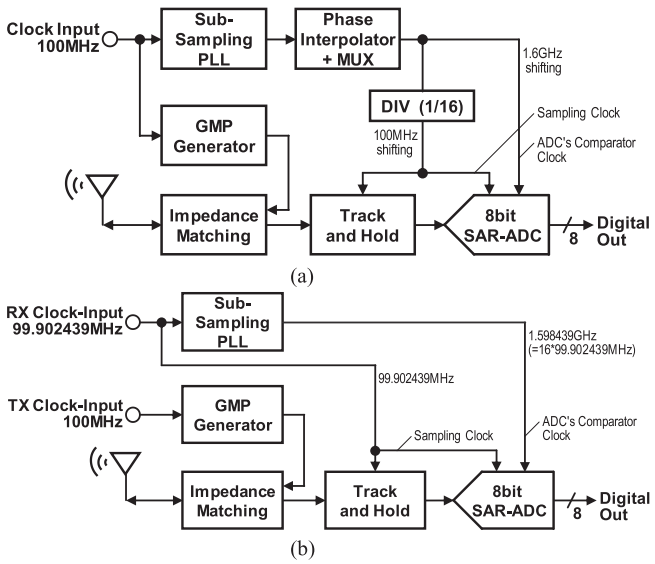


Fig. 6. Sampling clock generators. (a) Shifting clock. (b) Sliding clock

The measured phase noise versus offset frequency for the shifting clock with the sub-sampling PLL is shown in Fig. 7. A simulation result of the phase noise versus offset frequency is also plotted by a transient noise analysis, which is consistent with the measurement. The reference clock is generated by SG7050EBN. Although spurs due to non-linearity are observed in the frequency range of 10–100 KHz, the influence on the phase noise is negligible because of the lower frequency. The peaking observed at 10 MHz is attributed to the loop bandwidth, which

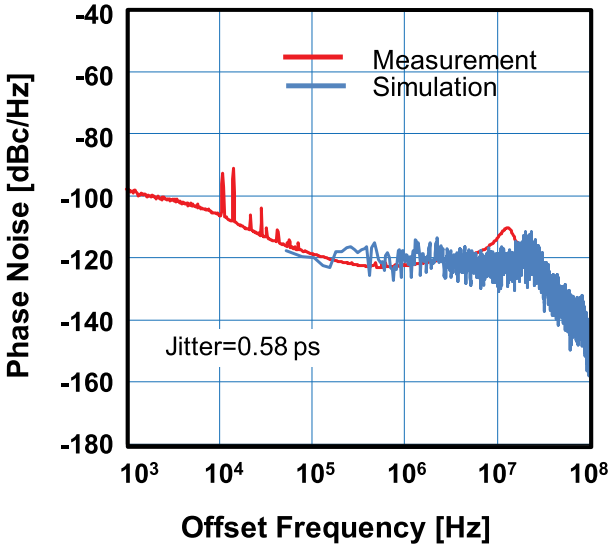


Fig. 7. Measured and simulated phase noises versus offset frequency for the shifting clock with sub-sampling PLL.

is consistent with the simulation result. The jitter is calculated from the phase noise by integrating from 1 KHz to 10 MHz of the offset frequency. The minimum measured jitter is 0.58 ps, whereas the simulated value is 0.42 ps.

On the other hand, the sliding clock is generated in the frequency domain by the beat of 100 MHz TX-clock and 99.902439 MHz RX-clock as shown in Fig. 6(b).

The reference clock frequency of TX-clock (KLO628MA) is 100 MHz, so that the frame period and the number of sampling points are 10 ns and 1024, respectively. The sampling resolution Δt is 9.765625 ps. The sliding clock frequency of RX-clock (KLO628MA) is 99.902439 MHz, which is calculated from 1/(10 ns+9.765625 ps). The maximum jitter of the crystal oscillator (KLO628MA) is 1.0 ps.

C. Track and Hold

In order to realize ultra-wide-band analog-to-digital signal processing for the scattered GMP with 200 ps pulse-width, a high-speed track and hold circuit with high gain and wide bandwidth is developed. A conventional passive T/H core has a drawback of low-pass characteristic during track-mode. The bandwidth of the active T/H core is wider than that of the passive structure because the switched-buffer works as current-domain sampling. However, it has some limitations in terms of both the large power supply noise due to rapid current changes and the limited bandwidth due to the hold capacitance during the track-mode.

To solve the problems, a proposed track and hold circuit is developed as shown in Fig. 8. It consists of an impedance matching (IM), a T/H buffer AMP1 (gain: 5.4 dB), a T/H core (gain: 9.4 dB), an output buffer AMP2 (gain: 8.3 dB), a DC cut (gain: 0 dB), and a variable gain amplifier (VGA) (gain: 0–10 dB).

The differential GMP signals with the bandwidth from 2.3 GHz to 8.2 GHz shown in Fig. 4 are transmitted from INP and

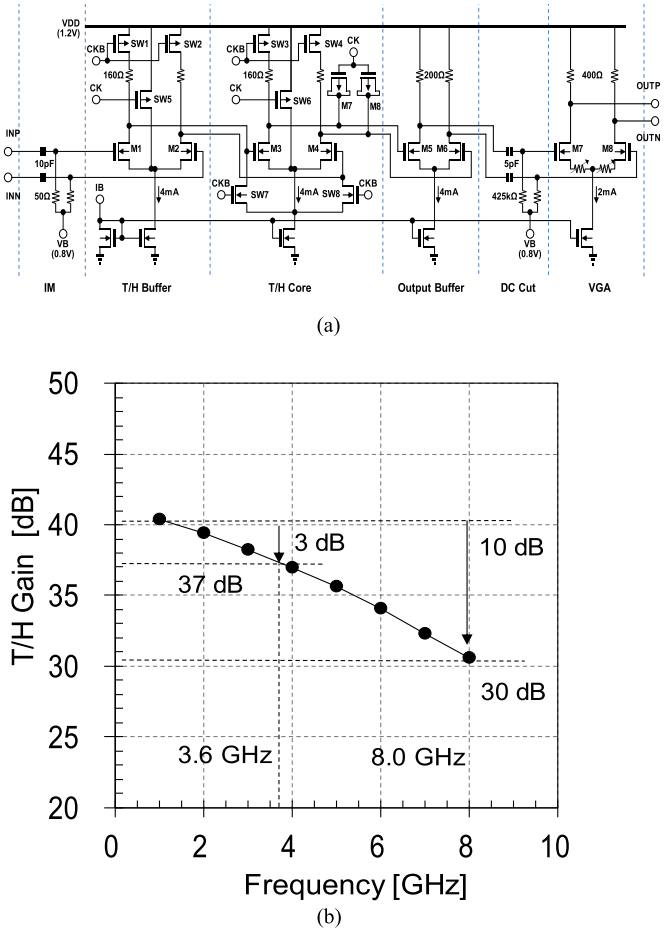


Fig. 8. (a) Schematic diagram of a differential T/H circuit. (b) Gain versus frequency for T/H circuit.

INN input ports to the input buffer of the differential track and hold circuit as shown in Fig. 8(a). It amplifies the GMP signal as the track mode when CK is high. Since the signal bandwidth becomes narrower when a hold capacitor for sampling exists, the gate capacitances of transistors M 5 and M 6 are used as the sampling capacitors. Removal of a hold capacitor is also effective for reducing power consumption.

When CK is low, transistors SW1-SW4 are turned off and the hold mode is set. The errors due to clock feedthrough and channel charge injection between the track and the hold modes cause offset voltages. To eliminate the errors, transistors M7 and M8 are used. Furthermore, transistors SW5 and SW6 are inserted as bypass switches. In the hold mode, the currents of T/H buffer and T/H core circuits stop. When the current suddenly stops, a large power supply noise occurs due to the parasitic inductance of a bonding wire. The current consumption changes dynamically and the power supply voltage has large noise without bypass switches. As a result, the sampling accuracy is deteriorated. When the bypass switches SW 5 and SW 6 are turned on and the current continues to flow in the hold mode, the sampling accuracy is improved.

Measured gain of the track and hold circuit as a function of frequency is shown in Fig. 8(b). The -3 dB and -10 dB bandwidths are 3.6 GHz and 8.0 GHz, respectively. The gain is

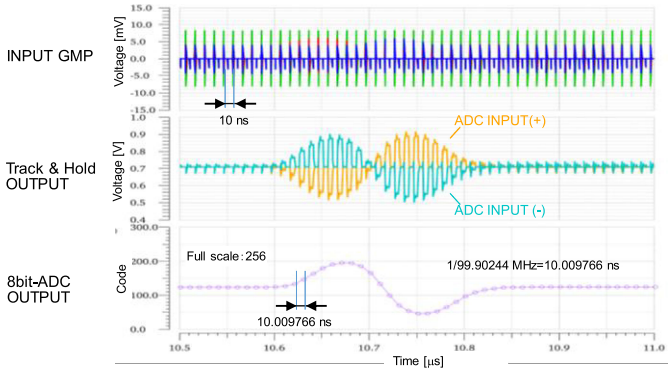
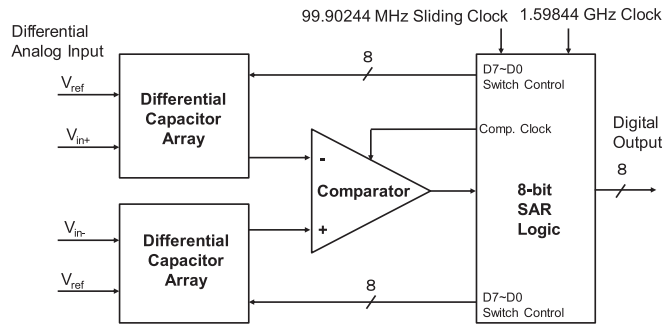


Fig. 9. Waveforms input GMP, T/H output, and 8-bit ADC output.



Design	Parameters
Resolution	8 [bits]
Sampling rate	99.902439 [MSPS]
Integral non-linearity (INL)	-7.1 ~ +1.2 [LSB]
Differential non-linearity (DNL)	-0.5 ~ +0.6 [LSB]
Unit capacitance	0.471 [fF]
Core area (8 bits)	0.011 [mm^2]

Fig. 10. Block diagram and design parameteres of 8bit-SAR-ADC.

30 dB at 8.0 GHz. Fig. 9 shows a simulation result of differential waveforms of GMP input, track and hold output, and 8-bit-ADC output in the sliding clock mode. The ADC output shows the effective sampling period of 10.009766 ns = 1/99.90244 MHz.

D. Analog-to-Digital Converter

After the track and hold circuit stage, the input differential GMP signals are converted to digital data by 8-bit SAR-ADC shown in Fig. 10. ADC design and parameters are tabulated. The 8-bit SAR-ADC starts to convert at every edge of given 99.902439 MHz sliding clock or 100 MHz shifting clock in the time domain. The internal SAR operation, including the sample and hold timing slot and the each-bit comparison operation, is clocked by 2/3 of the given 1.59844 GHz or 1.6 GHz clock.

Measured statistical distribution of the output code without signal input to the track and hold circuit and the 8-bit-SAR-ADC is shown in Fig. 11(a). The standard deviation of the output code for the 8-bit ADC including the track and hold circuit is 4.198 (code), which is equivalent to 19.8 mV. Since it is greater than 1 LSB (4.06 mV), the averaging of measurement data is necessary assuming that the standard deviation is attributed to

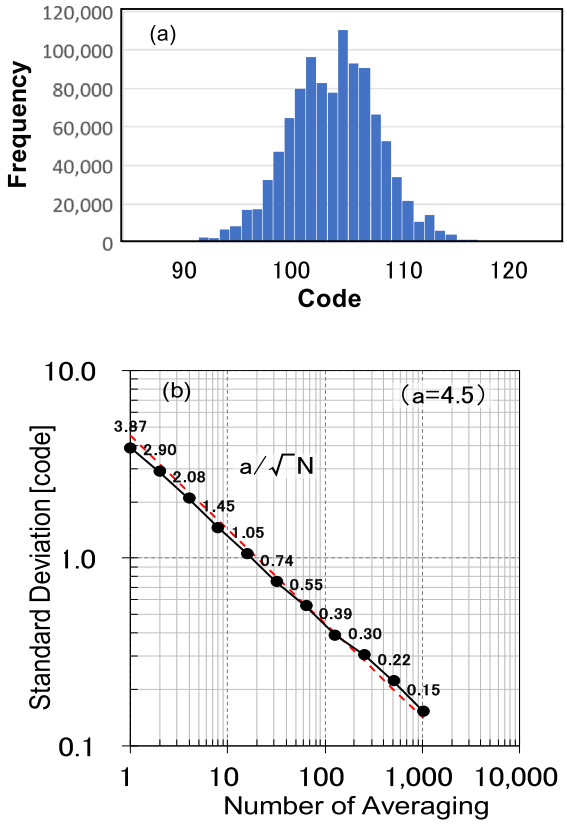


Fig. 11. (a) Measured statistical distribution of 8-bit ADC output without signal input to the track and hold circuit. (b) Measured standard deviation of the output code for the track and hold circuit plus 8-bit ADC as a function of the number of averaging.

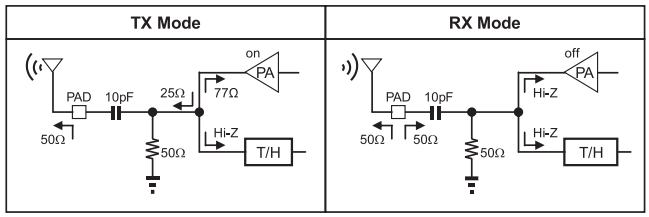


Fig. 12. Impedances of TX and RX ports in both states.

random noise. Measured standard deviation as a function of the number of averaging is shown in Fig. 11(b). It is correlated to the regression line of a/$\sqrt{N}$, indicating that the deviation is caused by random noise, where N is the number of averaging and the constant a = 4.5. Therefore, the averaging method for the measurement is adopted.

E. Ultrawideband-Input/Output

Fig. 12 shows the impedances of TX and RX ports for TX and RX modes. The maximum parasitic inductance of a bonding wire is 0.5 nH for the chip assembly so that the parasitic parallel capacitance is less than 100 fF. For the TX mode, the output impedance of the GMP generator circuit is 77 Ω. The generated GMP signal can be transmitted to the antenna via TX ports

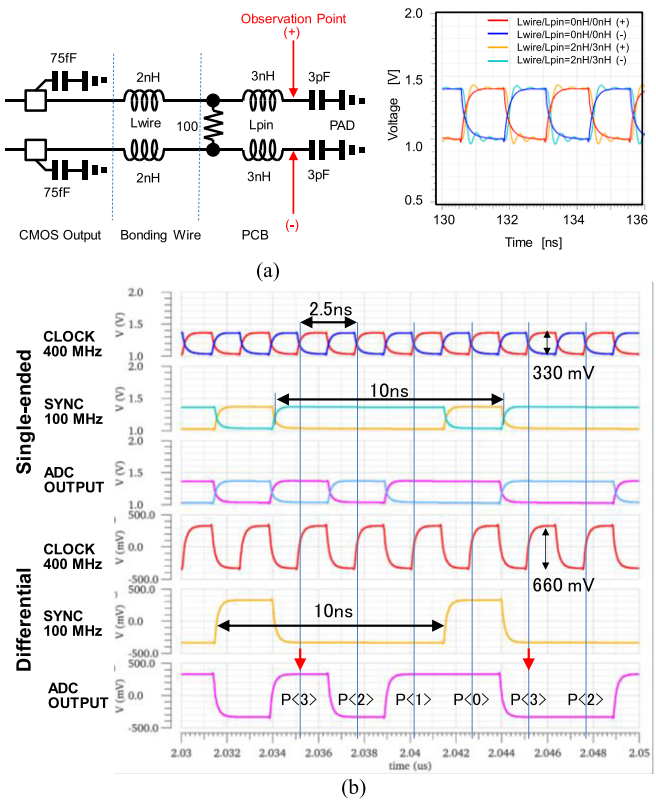


Fig. 13. Simulation results of LVDS driver. (a) Equivalent circuit of LVDS driver load and clock waveform. (b) ADC output with clock and synchronization pulse.

(UWBP / UWBN). For the RX mode, the received GMP signal from RX ports can be transmitted to the T/H.

Consequently, it is possible to switch between the transmission and the reception modes by directly connecting both the transmitter output and the receiver input into one port. When either the transmission or the reception circuit is in a stand-by mode, the corresponding port is sleeping. The 50 Ω resistor is used for the termination in the CMOS circuits because the wideband termination gives priority over the noise figure thanks to the noise reduction by averaging.

F. Low Voltage Differential Signaling

Since the GMP waveforms whose −3dB bandwidths are 5.9 GHz (2.3–8.2 GHz) and 4.2 GHz (1.7–5.9 GHz) are transmitted at the repetition rate of 100 MHz through I/O ports, low voltage differential signaling (LVDS) is adopted to keep the integrity. This is because the 8-bit-ADC output CMOS parallel buffer generates large currents in the silicon substrate and generates power-ground noise. Fig. 13(a) shows transient analyses of LVDS waveforms in terms of parasitic inductance dependence. The extracted inductances for bonding-wires and pins are 2 nH and 3 nH, respectively. The LVDS driver operates at 400 MHz clock with sufficient eye patterns. The 8-bit ADC output is converted to 2-bit data by the parallel-serial conversion. The ADC output with the clock and synchronizatin pulse is shown in Fig. 13(b).

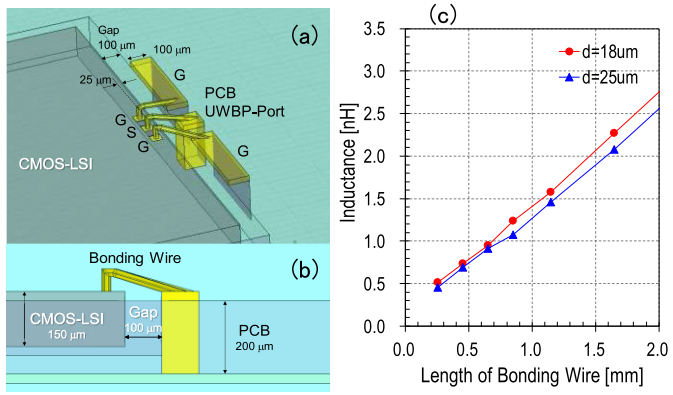


Fig. 14. Effect of bonding wire on parasitic inductance. (a) Bird's eye view of bonding wire. (b) Cross section vies of bonding wire. (c) Parasitic inductance versus length of bonding wire.

III. Fabrication and Characterization

A. GMP Transceiver Module

A wire-bonding technique is adopted to reduce the cost of fabrication. To reduce the parasitic capacitance and inductance of a bonding wire for UWB signal I/O ports, the length of the bonding wire is reduced. The parasitic capacitances and inductances of bonding wires were calculated by the electromagnetic analysis of S-parameters using HFSS. Fig. 14 shows parasitic inductance versus bonding wire length at 7 GHz. The shunt capacitance of a bonding wire is negligible. Figs. 14(a) and (b) are bird's eye and cross section views of bonding wires, respectively. Fig. 14 (c) shows calculated parasitic inductance versus length of bonding wire for different wire diameters. The parasitic capacitance of the bonding pad of CMOS-LSI is 60 fF for a pad with the size of 40 μm x 40 μm, which is calculated by LPE. Since the target parasitic inductance of a bonding wire is less than 0.5 nH, the length of bonding wire should be less than 0.25 mm. By taking into account of fabrication technology, the target length of bonding wire is set as 300 μm. To reduce the length of bonding wires for GMP I/O ports, the CMOS-LSI chip is counter sinking in the recessed substrate of the PCB as deep as 150 μm, which is equal to the thickness of the chip. A cross section diagram of a CMOS-LSI RF board is shown in Fig. 15. The dielectric properties of PCB cores for high frequency and low frequency interconnects are $\varepsilon/\tan\delta = 3.4/0.004$ (HL972) and $\varepsilon/\tan\delta = 4.4/0.021$ (CS-3665D), respectively.

Figs. 16 (a) and (b) show CMOS-LSI after wire bonding and RF board on which a CMOS-LSI is assembled. The chip size is 2.12 mm × 2 .22 mm and the device area is 1.74 mm × 1.84 mm. The power dissipations for transmitter and receiver circuits are 19.79 mW and 48.87 mW, respectively. The power consumption of the transceiver is reduced to approximately 1/25 in comparison with the prior prototype. A GMP radar module consists of printed circuit boards (PCB) of a CMOS-LSI RF board, a base board, and a FPGA board to realize smaller foot prints.

Figs. 17(a) and (b) show the front side of transceiver module (Base board + RF board) and the back side of transceiver module (Base board + FPGA board), respectively.

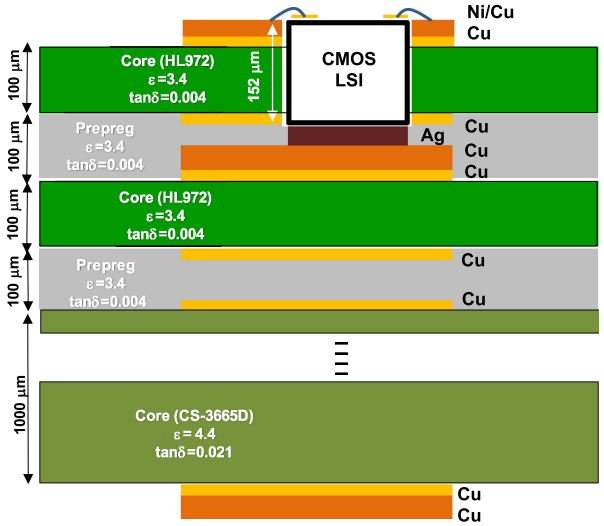
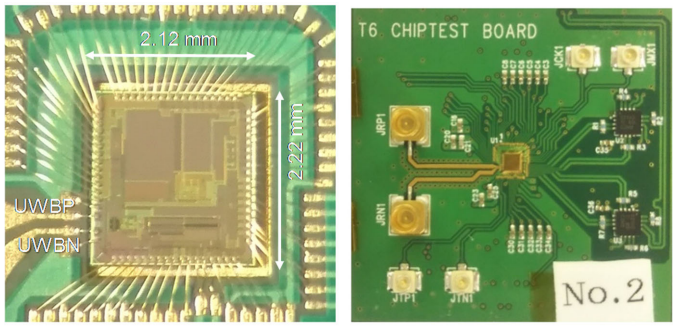
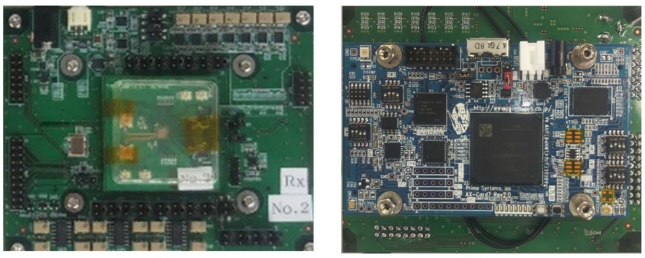


Fig. 15. Cross section diagram of CMOS-LSI RF board.



(a) (b)

Fig. 16. (a) Photomicrograph of CMOS-LSI after wire bonding. (b) Photograph of RF board on which CMOS-LSI is assembled.



(a) (b)

Fig. 17. Photographs of modules. (a) Front side of transceiver module (Base board + RF board). (b) Back side of transceiver module (Base board + FPGA board).

The FPGA board (Xilinx Artix-7 XC7A35TFGG484C-2) is assembled on the flip side of the base board. One module is set in GMP transmitter mode (TX), the other module is set in the receiver mode (RX).

Figs. 18(a) and (b) show block diagrams of GMP radar and FPGA modules, respectively. Since breast cancer tissues are found at the depths of 0.5–3 cm below a breast skin in a supine position, the distance is too close for the monostatic

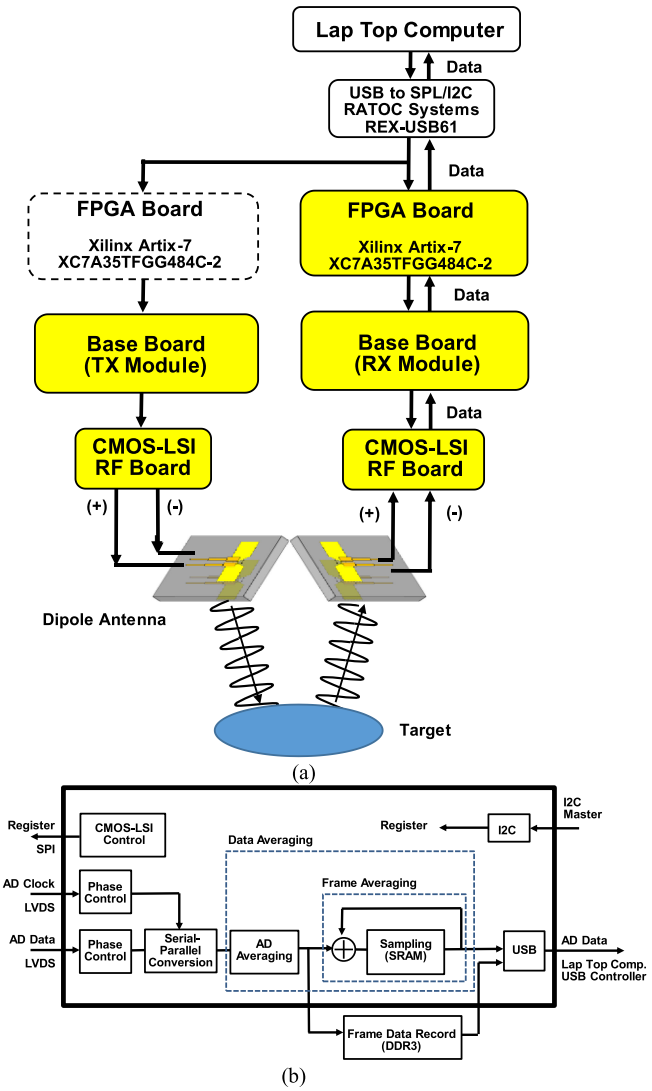


Fig. 18. Block diagram of a GMP bistatic radar module. (a) System block. (b) FPGA.

measurement to process the received signal. Therefore, the bistatic measurement is conducted to prevent the received signal from superimposing the emitting GMP signal. The relative advantage of the bistatic measurement using a single chip is the formation of multiple antenna array system without coaxial cables by miniaturizing the RF and Tx/Rx modules integrated on an antenna.

The transceiver base board can be used as either GMP transmitter (TX) module or receiver (RX) module. The FPGA board is assembled on the back side of the transceiver module for RX for serial-parallel conversion and averaging of ADC output data. The FPGA board mainly works for serial-parallel conversion and averaging of ADC output in GMP receiver mode (RX), so that FPGA board can be removed in GMP transmitter mode (TX). Differential GMP signals are generated by the CMOS-LSI RF board in TX mode and emitted from a transmitter antenna into a breast. The GMP is scattered at a cancer target, then the scattered signal is received by a receiver antenna.

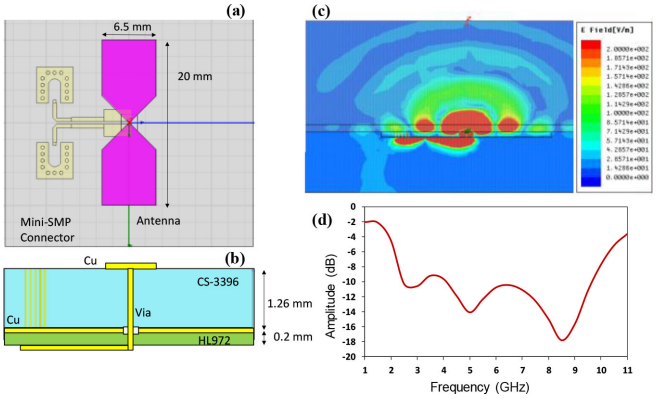


Fig. 19. Characterization of antenna. (a) Dipole antenna structure (plan view). (b) Dipole antenna structure (cross-section view). (c) Electric field radiation toward the human body. (d) Scattering coefficient (S11) versus frequency.

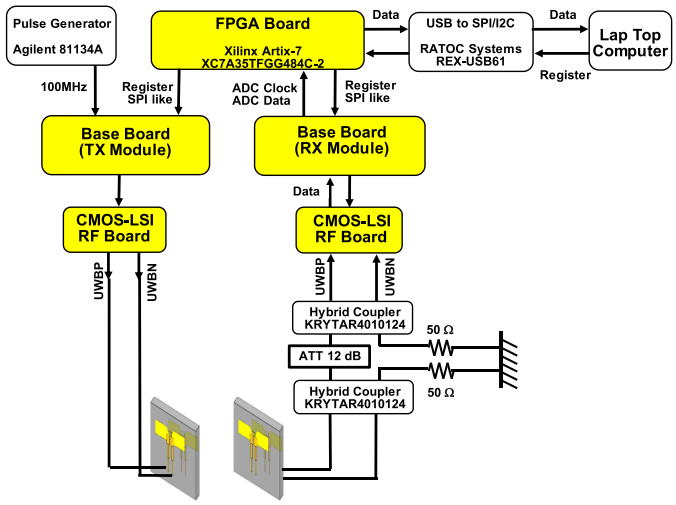


Fig. 20. Experimental setup for GMP transmission via dipole antennas.

B. UWB Dipole Antenna

Figs. 19(a), (b), (c) and (d) show a plan-view dipole antenna structure, cross-section view, electric field radiation and reflection coefficient (S11), respectively. High-k and low-k substrate materials are used for emitting UWB microwave into the breast through the skin and fat whose dielectric constants are approximately 20-30 and 4, respectively. The front side of the dipole antenna, which is closer to the skin, is RISHO CS3396 ($\varepsilon = 11.3$, $\tan\delta = 0.003$ @1 GHz) and the back side of the transmission line for an impedance transformer is HL972 ($\varepsilon = 3.4$, $\tan\delta = 0.004$ @12 GHz). The length and the width of the dipole antenna are 20 and 6.5 mm, respectively. The electric field radiation pattern is simulated by HFSS. The most of the power is radiated towards the breast which is perpendicular to the dipole antenna front plane. The electric field is radiated in the vicinity of the coplanar strip line on the backside but it does not expand further. The -10 dB bandwidth is divided into two frequency regions as 2.5–3.4 GHz and 4.0–9.6 GHz. The -9 dB bandwidth is 2.5–9.8 GHz.

C. GMP Transmission

GMP transmission experiments are conducted to verify the performance of the CMOS-LSI for microwave imaging. Fig. 20 shows an experimental setup for GMP transmission via dipole antennas. To mimick fat tissues in breasts, rubber sheets ($\varepsilon = 4$) with the thicknesse of 10 mm or 20 mm is inserted between the dipole antennas. Received waveforms of GMP transmission via coaxial cables are also measured so that the signal integrity of the CMOS-LSI can be evaluated.

The pulse widths, amplitude, -3dB bandwidths for the code_098_GMP are 286 ps, 325 mV pp (diff) and 4.2 GHz (1.7-5.9 GHz), respectively. The GMP is transmitted by the CMOS-LSI transceiver for TX module and received by that for RX module. The waveforms of the CMOS-LSI ADC output are compared with off-the-shelf sampling oscilloscopes (Agilent 86100C+86112A). The sampling periods Δt for the CMOS-LSI and the sampling oscilloscope are 9.77 ps and 7.41 ps, respectively. Measured waveforms of GMP transmission via coaxial cables are shown in Fig. 21. Figs. 21(a) and (b) show GMP waveforms that are received by the sampling oscilloscope

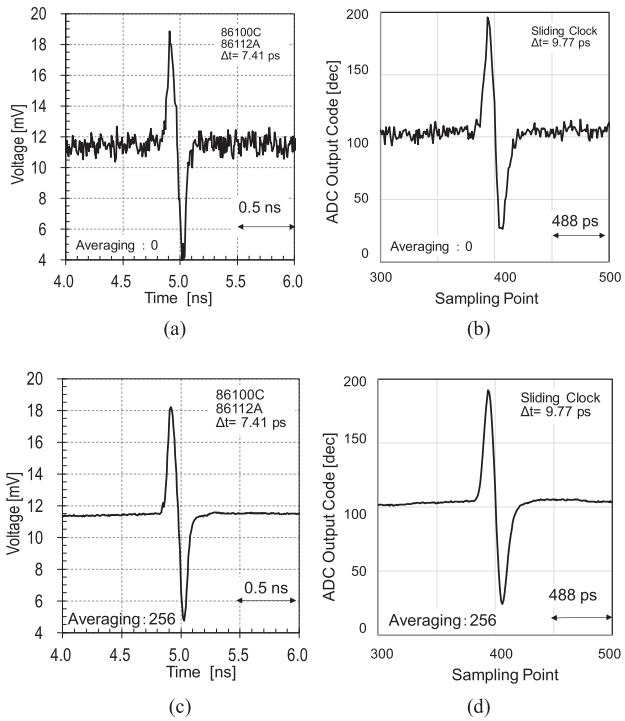


Fig. 21. Measured waveforms of GMP transmission via coaxial cable. (a) Sampling oscilloscope without averaging. (b) CMOS-LSI without averaging. (c) Sampling oscilloscope with 256-time averaging. (d) CMOS-LSI with 256-time averaging.

without averaging and by the CMOS-LSI transceiver for RX without averaging, respectively. Figs. 21(c) and (d) show GMP waveforms which are received by the sampling oscilloscope with averaging of 256-times and the CMOS-LSI transceiver for RX with averaging of 256-times, respectively. It is found that the GMP waveforms of the CMOS-LSI transceiver for RX are similar to those of the sampling oscilloscope.

Measured waveforms of GMP transmission via the dipole antennas are shown in Fig. 22. Figs. 22(a) and (b) show GMP

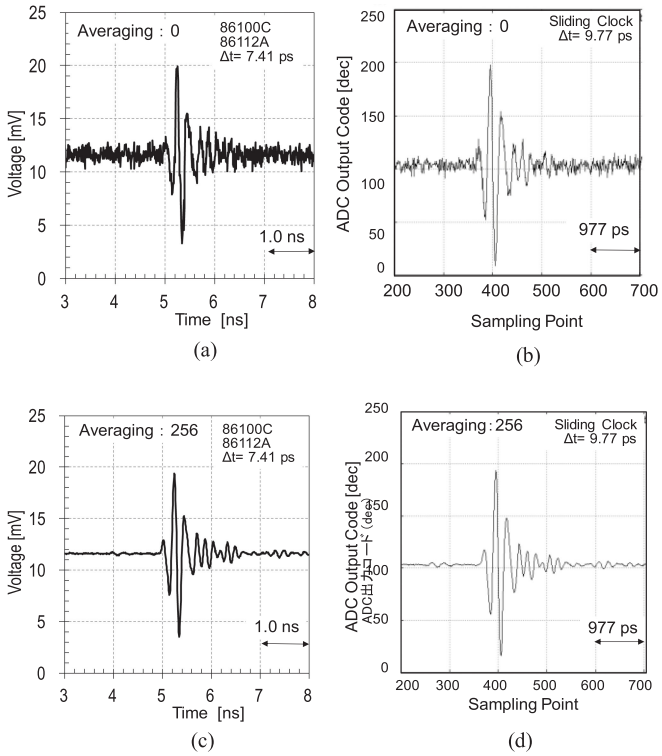


Fig. 22. Measured waveforms of GMP transmission via dipole antennas. (a) Sampling oscilloscope without averaging. (b) CMOS-LSI without averaging. (c) Sampling oscilloscope with 256-time averaging. (d) CMOS-LSI with 256-time averaging.

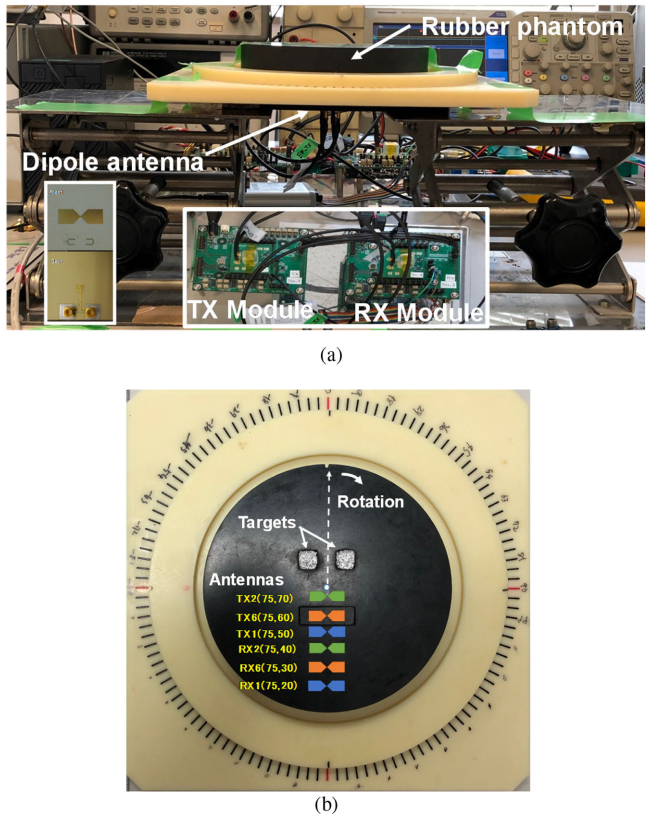


Fig. 23. Measurenment setup for confocal imaging. (a) Photograph of experimental set-up. (b) Antenna coordinates.

waveforms that are received by the sampling oscilloscope without averaging and by the CMOS-LSI transceiver for RX without averaging, respectively. Figs. 22(c) and (d) show GMP waveforms that are received by the sampling oscilloscope with averaging of 256 times and the CMOS-LSI transceiver for RX with averaging of 256 times, respectively. It is found that the GMP waveforms of the CMOS-LSI are consistent with those of the sampling oscilloscope.

D. Confocal Imaging

Fig. 23 shows a measurement setup for confocal imaging. Two phantom targets (10 mm × 10 mm × 5 mm) with a spacing of 10 mm are buried in a rubber phantom (diameter: 132 mm, thickness: 40 mm). The dielectric constants of the targets and the surrounding media are approximately 70 and 4, respectively. Three channels of TX and RX dipole antenna pair are located as shown in Fig. 23(b). The target is located at the depth of 23 mm from the antenna surface. Measurement was carried out by rotating the phantom from 0 to 360 degrees at 9-degree step, where TX and RX antennas are fixed. The detail of the confocal imaging algorithm is published in the reference [23]. A plan view and a cross section view of two phantom targets are reconstructed by the confocal imaging as shown in Figs. 24(a) and (b), respectively. Three-dimensional image of the two targets is shown in Fig. 24(c). The signal-to-clutter ratio (SCR) and signal-to-mean ratio (SMR) are 1.25 dB and 20.79 dB, respectively. The SCR is not significant due to multiple targets. The confocal images with the resolution of 1 cm can be reconstructed using the developed CMOS GMP transceiver LSI.

IV. Discussion

To investigate the noise characteristics, simulation and measurement for SNR and signal-to-noise and distortion ratio (SNDR) of the receiver (T/H+ADC) including the parasitic inductance of wire-bonding were carried out. Fig. 25 shows the transient noise analyses in the circuit blocks of T/H buffer and T/H core. The noise is generated in the T/H buffer during the tack and hold mode so that the noise is transmitted to the T/H core. The degradation in SNR, SNDR and effective number of bits (ENOB) for the receiver is attributed to the noise generated in the T/H-buffer as well as the thermal noise in the input transmission line impedance due to its large bandwidth. The thermal noise voltage generated in the input resistance is $V_n = \sqrt{4kTRB} = 69.8\ \mu\mathrm{Vrms}$, where Boltzmann constant *k,* temperature *T, r*esistance *R,* GMP bandwidth *B* are 1.38×10^{-23} JK^{-1}, 300°K, 50 Ω and 5.9 GHz, respectively.

Fig. 26 shows measured and simulated SNR and SNDR as a function of input voltage for the receiver. When the input signal voltage is 7.07 mVrms (−30 dBm), the simulated values of SNR and SNDR are 30 dB and 28 dB, respectively. The difference between simulation and measurement is about 10 dB shift of the

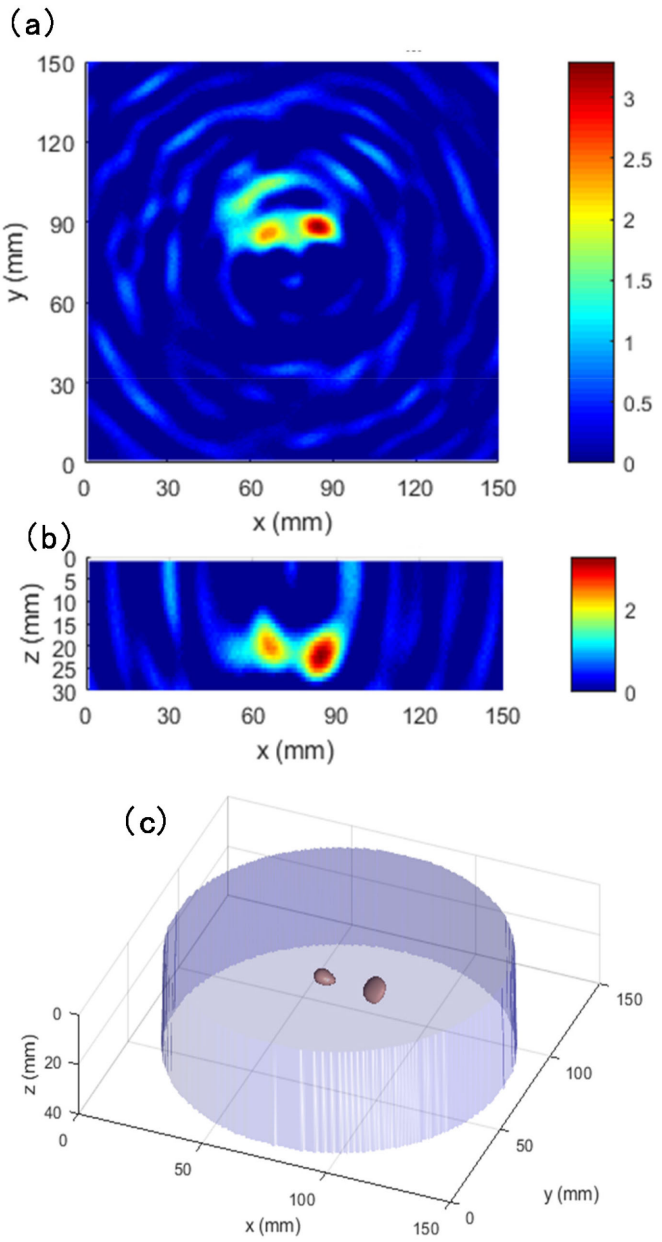


Fig. 24. Confocal images of two phantom targets. (a) Planview of the maximum confocal image. (b) Cross section image of the maximum confocal image. (c) Three dimensional image of two phantom targets.

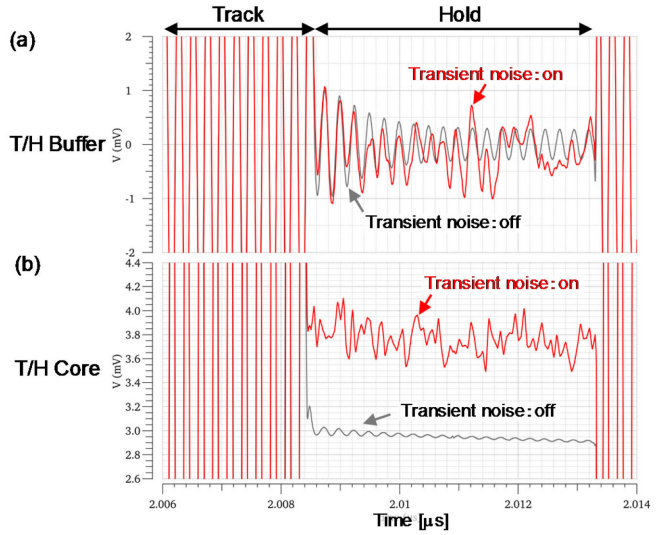


Fig. 25. Transient noise analyses in T/H buffer and T/H core circuit blocks. (a) T/H buffer. (b) T/H core.

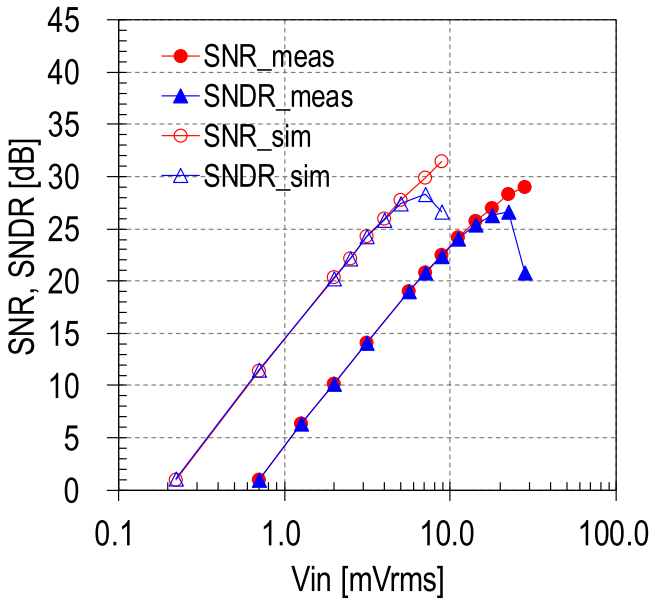


Fig. 26. Measured and simulated SNR and SNDR versus input voltage for T/H-ADC.

input voltage, which is due to the difference of the estimated gain of the T/H core. The measurement results of SNR, SNDR and ENOB at the input voltage of 22 mVrms (−20 dBm) for the equivalent bandwidth of 51.2 GHz are 28.4 dB, 26.6 dB and 4.1 bits, respectively. The measured SNR for the receiver bandwidth of 3.6 GHz is 36.3 dB. The noise figure (NF) is estimated at 12 dB by a S-parameter analysis. The degradations of SNR and SNDR in the bandwidth of 51.2 GHz are attributed to the thermal noise generated in the T/H buffer so that it must be reduced by increasing the current in the T/H buffer circuit.

The figure of merit (FOM) of 38 [fJ/conv] is obtained for the sampling frequency of 102.4 GHz using the equation of FOM = Power/[$2^{\mathrm{ENOB}} \times 2 \times \mathrm{B}$]. The input referred noise voltage without averaging is 0.24 mVrms. It can be reduced to 0.0053 mVrms after averaging of repeated measurement by 2048 times (0.24 mVrms/$\sqrt{2048}$). The averaging is not a significant penalty for 100 MHz clock because the averaging time is as short as 10 ns × 1024 points × 2048 times = 21 ms. It has been confirmed that the averaging of 2048-times repeated measurement is acceptable for the pilot clinical test at the hospital for breast cancer detection [16].

Table II summarize the performance of the developed CMOS GMP transceiver in comparison with the state of the art. This CMOS-LSI has both TX (GMP transmitter) and RX (8-bit-SAR-ADC) for a radar imaging application. The relative advantages

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART

	This Work (GMP+T/H+ADC)	ISSC 2019 [24]	ISSCC 2010 [25, 26]	ISSC 2016 [27]	ISSCC 2013 [28]	JSSC2015 [29]
Radar Type	UWB	FMCW	FMCW	FMCW-SAR	N/A	N/A
Spatial Resolution [cm]	1.0	1.1	21.4	11.2	N/A	N/A
Technology [nm]	CMOS-65	CMOS-28	CMOS-65	CMOS-65	CMOS-65	CMOS-65
Supply Voltage [V]	1.2	1.4	1.2	1.2	1.0	1.0
Area [mm^2]	0.56	6.5	1.045	4.06	1.82	2.0
Power [mW]	68.7	500	243	259.4	76	88.2
TX Frequency [GHz]	5.2 (Center)	145	75.6-76.3	15	N/A	4.7
Band-width [GHz]	5.9 (GMP)	13	N/A	N/A	N/A	N/A
Pulse-width [ps]	192 (GMP)	N/A	N/A	N/A	N/A	N/A
RX ADC Resolution [bits]	8	N/A	N/A	10	10	8
Sampling Frequency [GHz]	0.1 / 102.4	N/A	N/A	N/A	0.01 / 130	0.08 / 666
Sampling Period [ps]	10	N/A	N/A	N/A	6.25	1.5
Clock Jitter [ps]	0.58	N/A	N/A	N/A	8	N/A
Bandwidth [GHz]	3.6 / 51.2	13	0.7	1.5	7.3	8
SNR [dB]	36.3 / 28.3	N/A	N/A	N/A	N/A	N/A
SNDR [dB]	26.6	N/A	N/A	N/A	27	42 (8192 avg.)
ENOB [bits]	4.1	N/A	N/A	N/A	4.2	7.3 (8192 avg.)
Gain [dB]	30	80	38.7	3-58	12	N/A
Noise Figure [dB]	12	8	7.4	5.6-6.3	4	N/A
Input Referred Noise [mVrms]	0.24	N/A	N/A	N/A	N/A	N/A
FoM (Sampling Freq.) [fJ/conv.]	38	N/A	N/A	N/A	N/A	N/A

UWB: ultrawideband radar, FMCW: Frequency modulated continuous wave radar, SAR: Synthetic aperture radar
GMP: Gaussian monocycle pulse, T/H: track and Hold, ADC: Analog-to-digital converter.

of this work are the improved spatial resolution (<1 cm) with the 102.4 GHz ETS, the reduced jitter (0.58 ps) and the reduced power consumption (68.7 mW). To the best of our knowledge, this is the first demonstration of a single chip IR-UWB-CMOS radar for microwave imaging.

V. CONCLUSION

A single chip Gaussian monocycle pulse transceiver CMOS-LSI for UWB radar-based microwave imaging was developed. It achieves both GMP transmission with 192 ps pulse-width in the TX-mode and 102.4 GS/s effective time sampling of 8-bit-SAR-ADC with the clock jitter of 0.58 ps in the RX-mode. The total power consumption is 68.66 mW. Confocal imaging of a breast phantom is demonstrated using TX and RX modules with dipole antennas. The GMP transceiver module can differentiate two phantom targets with the size of 1 cm and the spacing of 1 cm in the near field, showing the potential for breast cancer imaging with a single-chip CMOS-LSI.

ACKNOWLEDGMENT

The authors would like to thank Prof. Morihito Okada and Prof. Koji Arihiro, Hiroshima University Hospital, for their helpful suggestions and supports. We also would like to thank Mr. Hiromasa Watanabe for his technical support.

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